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FUSION

(MS-7702L2 Ver:1.0) mATX: 244mm * 244mm

CPU:

AMD FM1(Llano uPGA FAMILIES)

System Chipset:

AMD - Hudson D3/D2

On Board Chipset:

CLOCK GEN --FCH internal clock gen

LPC Super I/O --NCT6776F

LAN-Realtek 8111E/8105E

Azalia CODEC - Realtek ALC892/662/888/

Main Memory:

DDR III * 4 (max 32G)

Expansion Slots:

PCI Express X16 Slot * 1

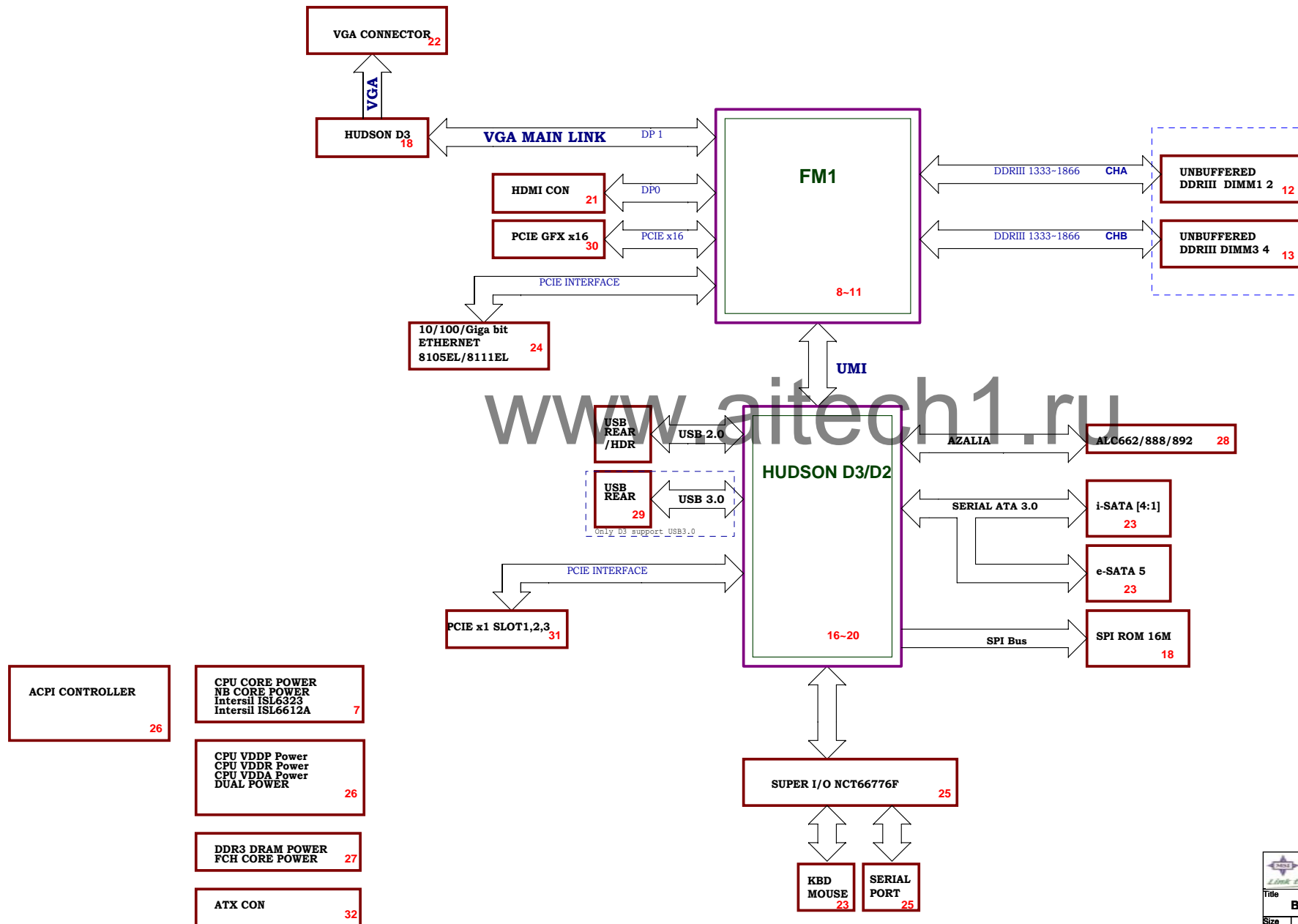
PCI Express X1 Slot * 3

PCI Express X1 Slot *1 for front USB3.0

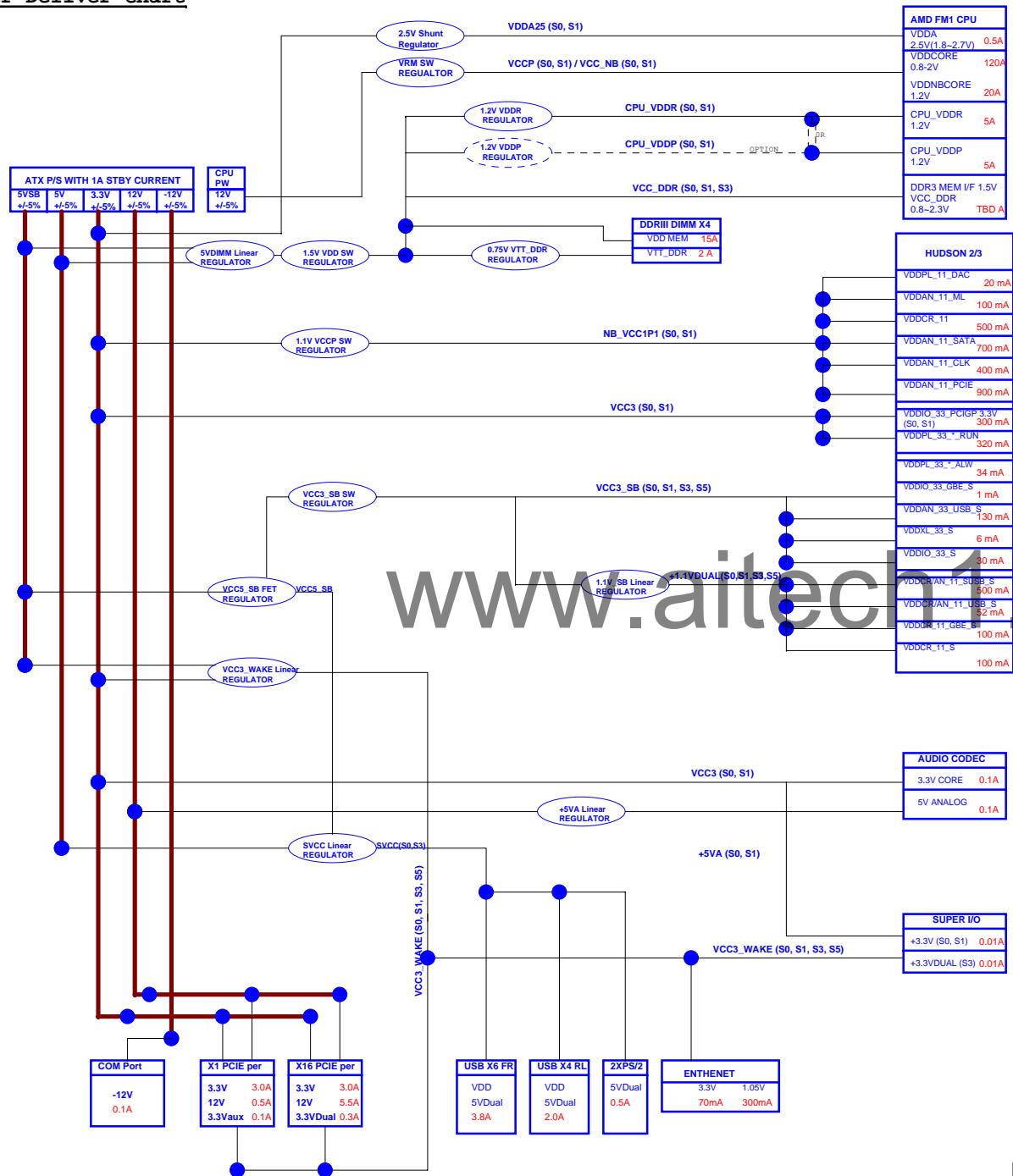
VRM

Controller - Intersil 6328 3+1 Phase

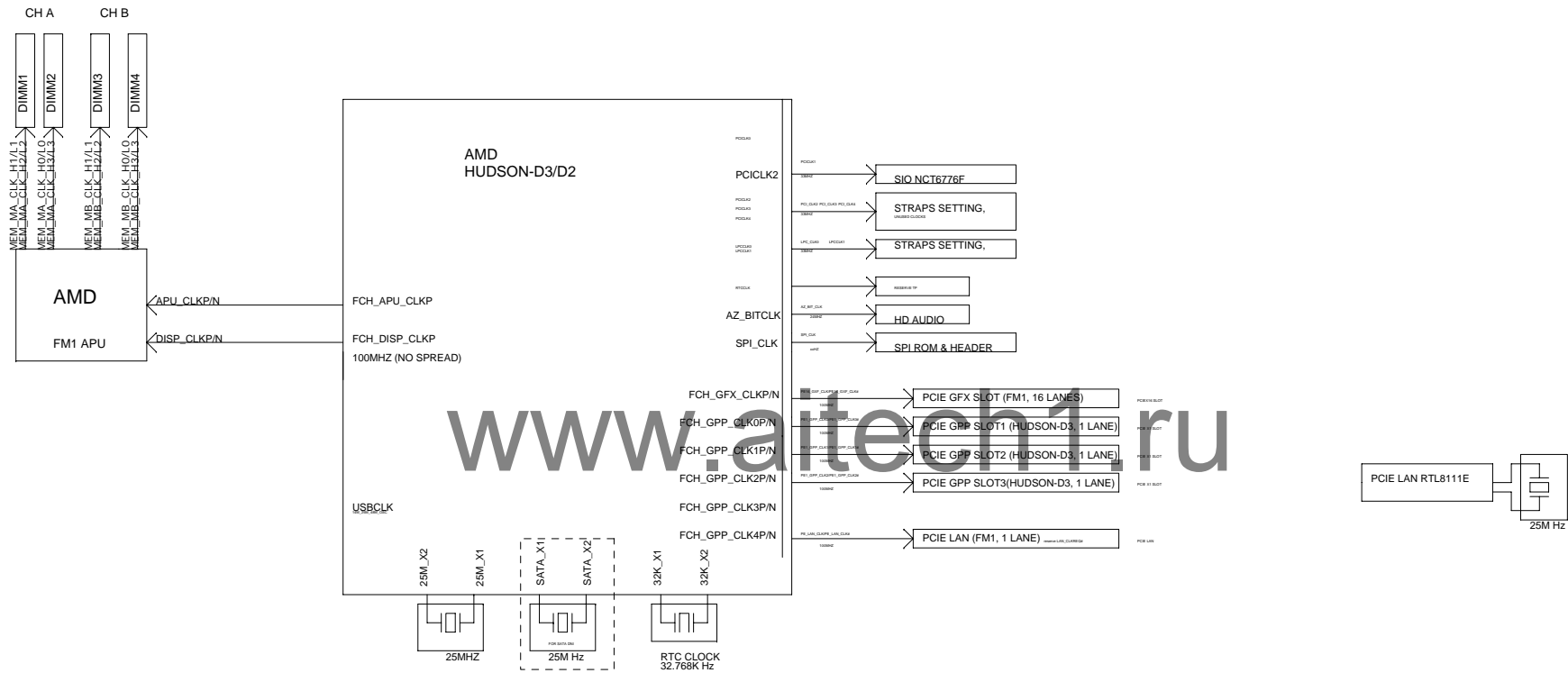
FUSION BLOCK DIAGRAM



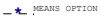
Power Deliver Chart



INTERNAL CLOCK MODE

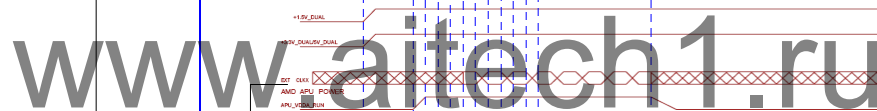


PWRGD MAP



RESET MAP

POWER ON SEQUENCE



SIO NCT6776F GPIO Config

Pin	GPIO	Power Rail	Function description	Comment
38	GP46	VSB	SIO_WAKE	
39	YLW_LED/GP45	VSB	SUS_LED	reserved
40	GRN_LED/GP44	VSB	PWR_LED	
42	GP67	VSB	USB_EN	OD
44	GP65	VSB	MB_ID0	GPI reserved
45	GP64	VSB	MB_ID1	GPI reserved
47	GP63	VSB	MB_ID2	GPI reserved
48	GP62	VSB	COM_GPIO2	GPI
49	GP61	VSB	CHASSIS_ID1	GPI reserved
50	GP60	VSB	CHASSIS_ID2	GPI reserved
78	GP36	VSB	SIO_VDUAL_EN	

FCH HUDSON D3/D2GPIO Config

Pin	pin Name	Function description
AJ3	AD0/GPIO0	CLEAR_CMOS
J2	IR_LED#/LLB#/GPIO184	MINI_PWRON
AD22	SATA_ACT#/GPIO67	SATA_LED#:SATA Channel Active
M6	TEMPIN3/TALERT#/GPIO174	FCH_TALERT#:Thermal Alert. The FCH can be programmed to generate an SMI, SCI, or IRQ13 through GPE, or generate an SMI without GPE in response to the signal's assertion.
V3	SPI_CLK/GPIO162	SPI Clock
V6	SPI_DI/GPIO164	SPI Data In
V5	SPI_DO/GPIO163	SPI Data Output
T6	SPI_CS1#/GPIO165	SPI Chip Select1#
V1	ROM_RST#/SPI_WP#/GPIO161	SPI write protect (active low)
Y6	SPI_HOLD#/GEVENT9#	SPI HOLD#. Assert low to hold the SPI transaction.
T8	USB_OC0#/SPI_TPM_CS#/TRST#/GEVENT12#	OC#0:USB 3.0 port 3,USB 2.0 port 13
J7	USB_OC1#/TDI/GEVENT13#	OC#1:USB2.0 port 4,5
P5	USB_OC2#/TCK/GEVENT14#	OC#2:USB2.0 port 8,9
P5	USB_OC3#/AC_FRES/TDO/GEVENT15#	OC#3:USB 3.0 port 0,USB 2.0 port 10
P6	USB_OC4#/IR_RX0/GEVENT16#	OC#4:USB 3.0 port 1,USB 2.0 port 11
T1	USB_OC5#/IR_TX0/GEVENT17#	OC#5:USB2.0 port 2,3
R8	USB_OC6#/IR_TX1/GEVENT6#	OC#6:USB2.0 port 0,1
M7	BLINK/USB_OC7#/GEVENT18#	OC#7:USB 3.0 port 2,USB 2.0 port12
	GPIO[171::173];GPIO[175::182];GPIO[193::194]	Configure as one of the following: 10-kΩ 5% pull-up resistor to +3.3V_S5. 10-kΩ 5% pull-down resistor.

DDR DIMM Config.

DEVICE	ADDRESS	CLOCK
DIMM 1 CH-A	10100000B A0H	MEM_MA_CLK_H1/L1 MEM_MA_CLK_H2/L2
DIMM 2 CH-A	10100010B A4H	MEM_MA_CLK_H0/L0 MEM_MA_CLK_H3/L3
DIMM 3 CH-B	10100001B A2H	MEM_MB_CLK_H1/L1 MEM_MB_CLK_H2/L2
DIMM 4 CH-B	10100011B A6H	MEM_MB_CLK_H0/L0 MEM_MB_CLK_H3/L3

SMBus TABLE

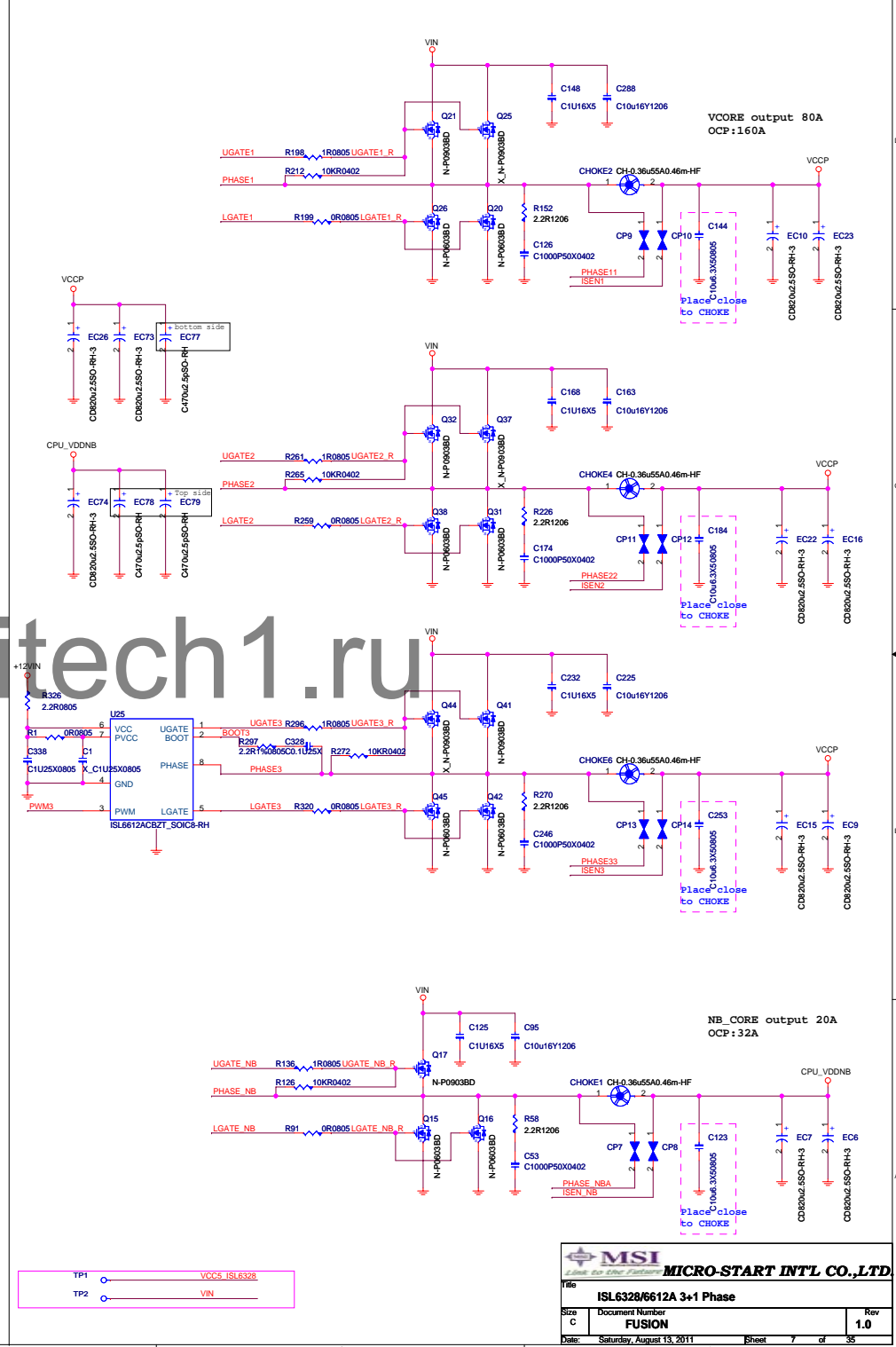
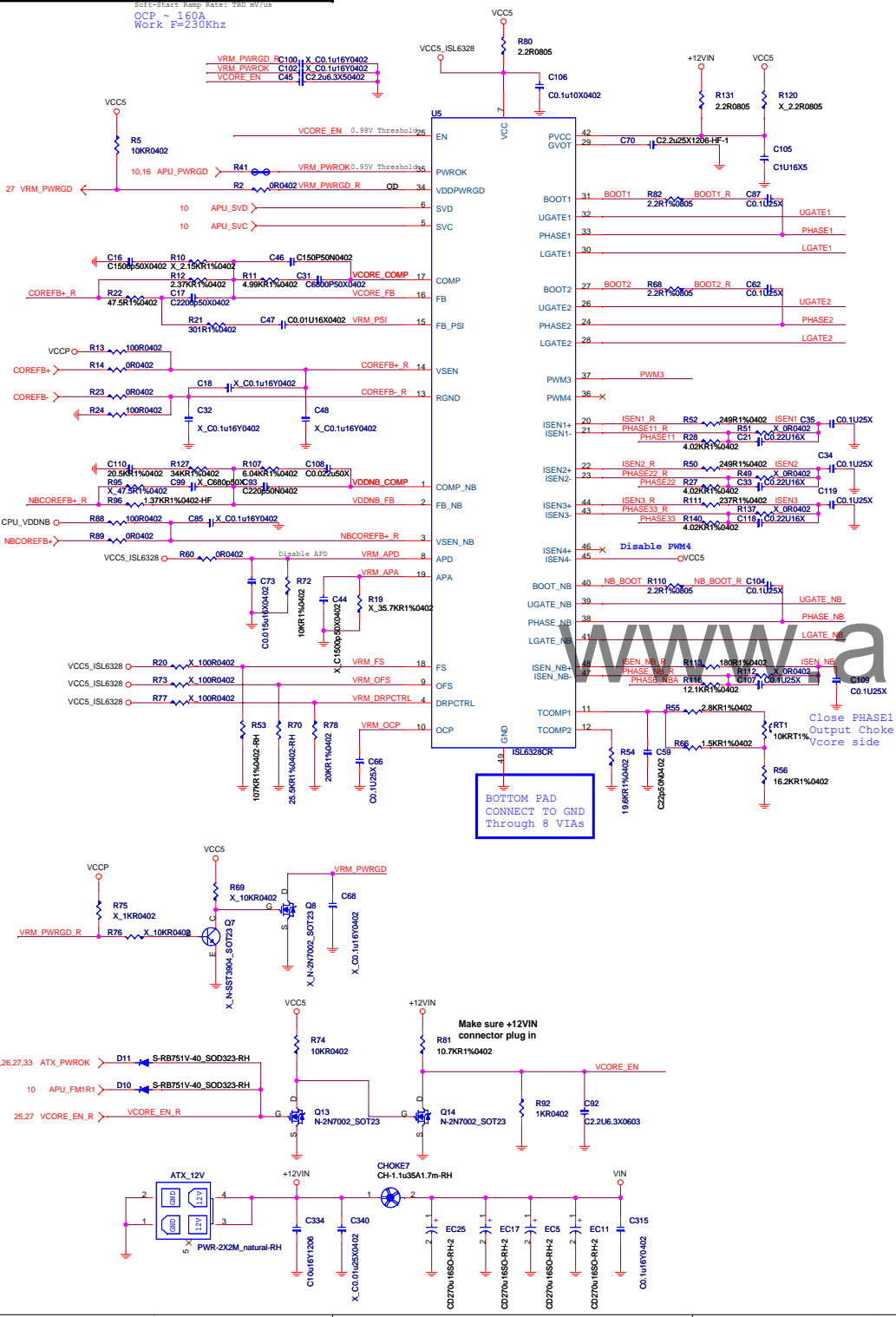
SOURCE	SINGLE NAME	LINKED DEVICE
APU	DPO_AUXP_C /DPO_AUXN_C	HDMI
	DP1_AUXP_C /DP1_AUXN_C	Hudson D2/3 DP to VGA translator
FCH	SCLK0/SDATA0	DIMMs,CLOCK GEN ,SIO
	SCLK1/SDATA1	LAN,PCIE SLOTS,MINI_PCIE
	SCLK3/SDATA3	TP

RESET TABLE

SOURCE	SINGLE NAME	LINKED DEVICE
FCH	PCIE_RST#	PCie 16X,1X,LAN,MINI_PCIE
	A_RST#	SIO,LPC debug
	PCIE_RST2#	RESERVE TP
	LDT_RST#	APU
	AZ_RST#	AZALIA CODEC
	DDR3_RST#	NC
	FC_RST#	DEBUG BUS
	ROM_RST#	NC
FRONT PANEL	FP_RST#	FCH,CLOCK GEN

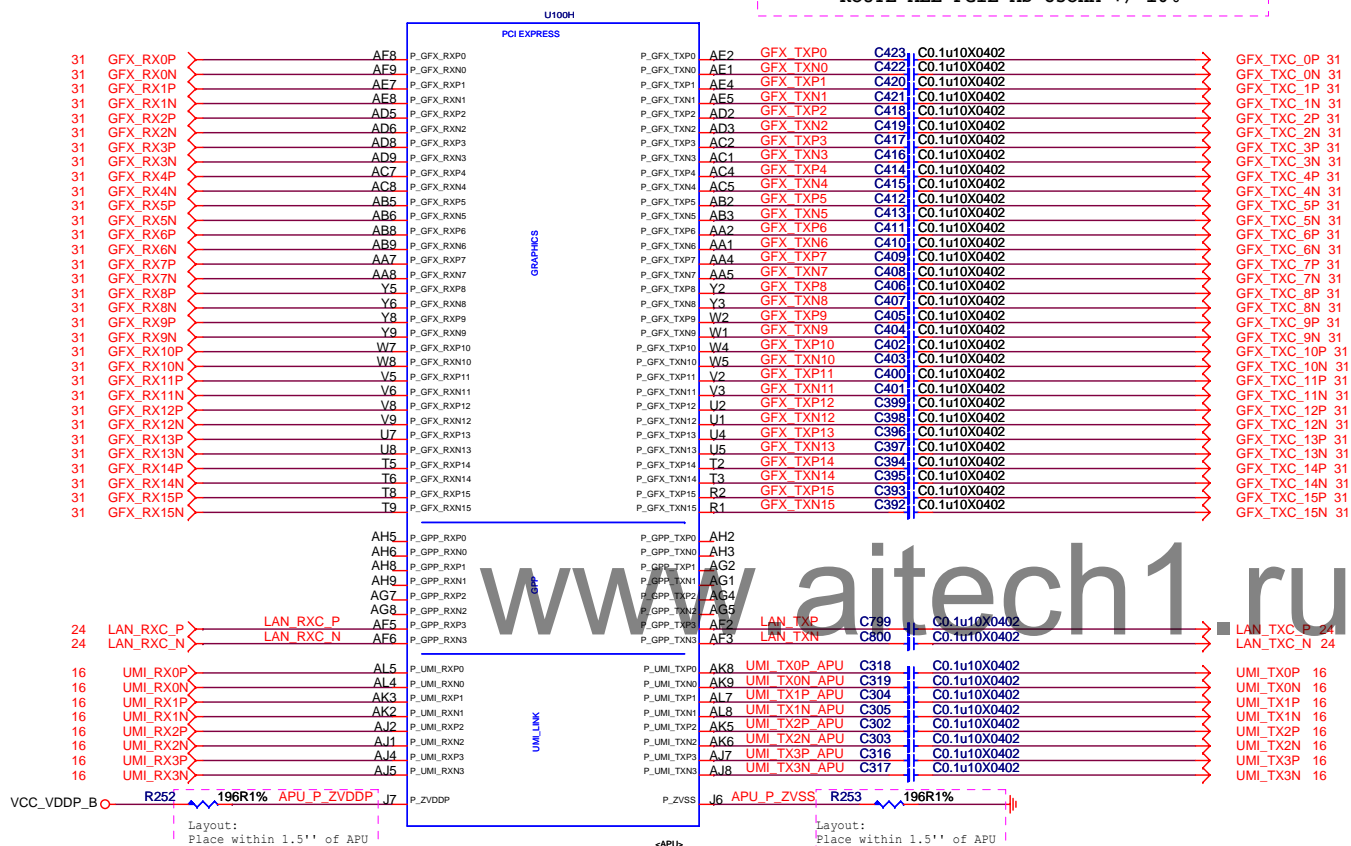
ISL6328/6612A 3+1 Phase

Soft-Start Ramp Rate: 7
OCP ~ 160A
Work F=230Khz



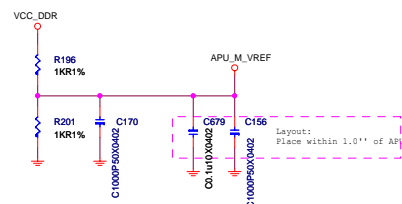
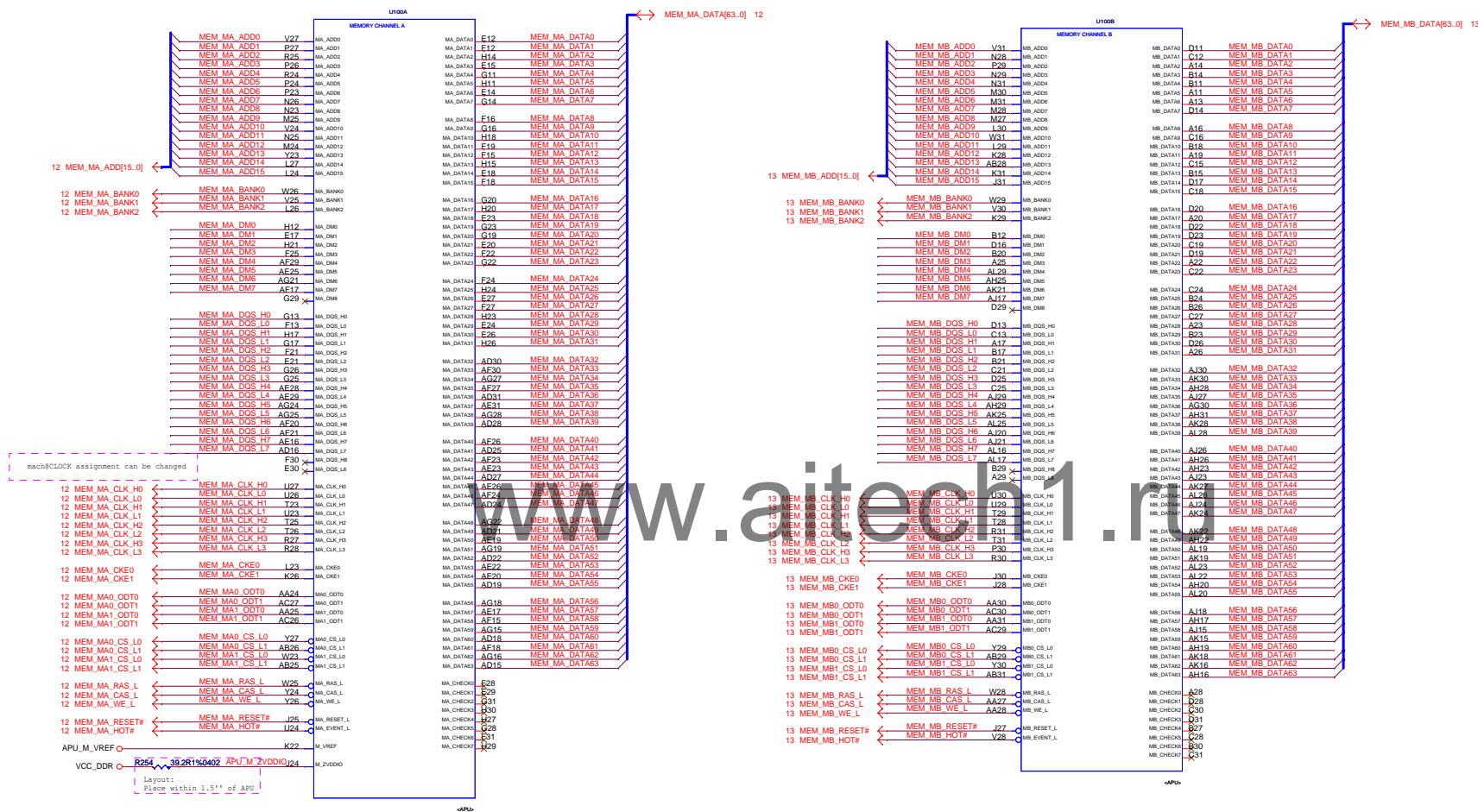
FM1 PCIE I/F

mach@CRB PCIE AC Capacitors:75nF to 200nF
Layout: PLACE CAPS WITH APU < 1 INCH
ROUTE ALL PCIE AS 85OHM +/-10%



12 MEM_MA_DQS_L[7..0] ↔
12 MEM_MA_DQS_H[7..0] ↔
12 MEM_MA_DM[7..0] ↔

13 MEM_MB_DQS_L[7..0] ↔
13 MEM_MB_DQS_H[7..0] ↔
13 MEM_MB_DM[7..0] ↔



Note: Several vias on the DPO interface violate the minimum distance rules for via to via spacing between diff pairs. These violations have been reviewed and approved on an individual basis, and pose no significant signal integrity issues for this implementation since the route lengths are under the maximum allowed spec, and the via distance violations are not severe.

U100C

ANALOGDISPLAYMSC

DP0_TXP0

DP0_TXN0

DP_AUX_ZVSS

DP_AUX_ZVSS

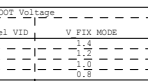
R207

150R1%0402

Layout: Place within 1.5" of APU



TEST2, TEST3, TEST6, TEST10, TEST23, TEST28 H TEST28 L, and any RSVD pins have no connections. TEST4, TEST5, TEST[17:14], TEST25 H/L, TEST30 H/L, and TEST32 H/L have onboard test points.

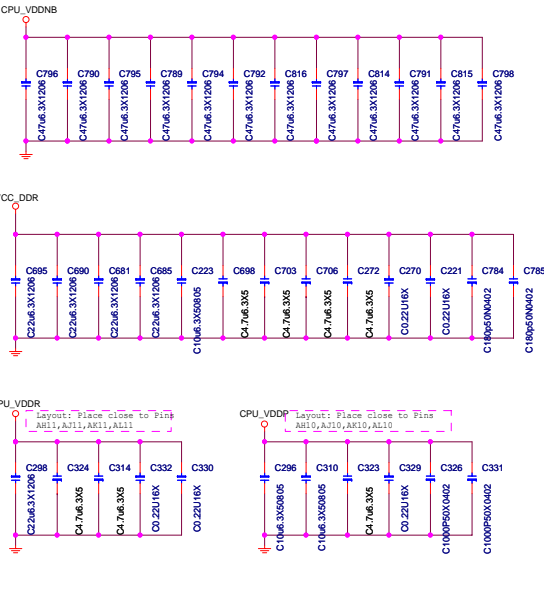
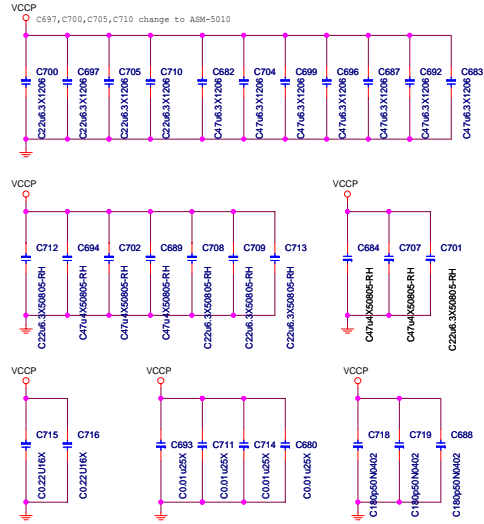


VCC_DDR Layout: Place close to HDT header

RE53	1KR0402	CPU_TDI
RE51	1KR0402	CPU_TCK
RE52	1KR0402	CPU_TMS
RE57	1KR0402	CPU_TRST_L
RE54	300R0402	CPU_DBREQ_L

Diagram illustrating the structure of the TP79 and TP8-TP32 gene clusters. The TP79 gene is shown as a single unit with two exons. The TP8, TP7, and TP32 genes are shown as a cluster, each with two exons. The genes are color-coded: TP79 is red, TP8 is blue, TP7 is green, and TP32 is orange. The exons are represented by boxes, and the introns by lines. The genes are arranged in a linear fashion, with TP79 at the top and TP8, TP7, and TP32 below it.

BOTTOM SIDE DECOUPLING

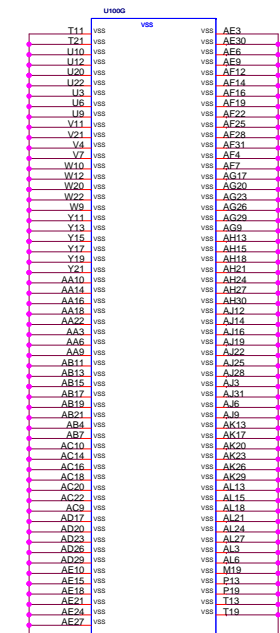
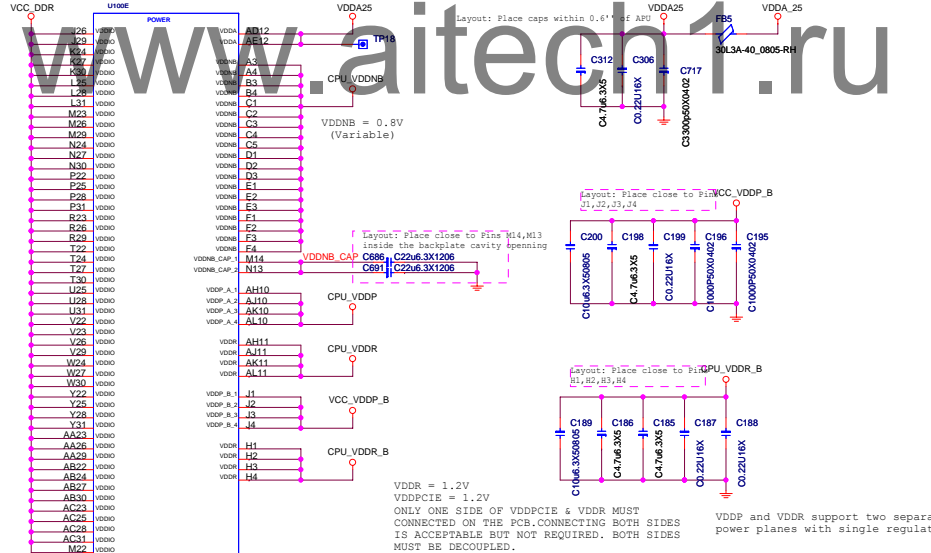
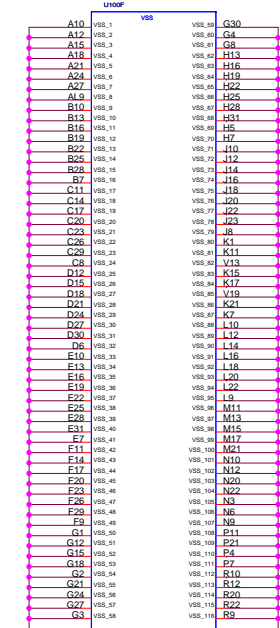
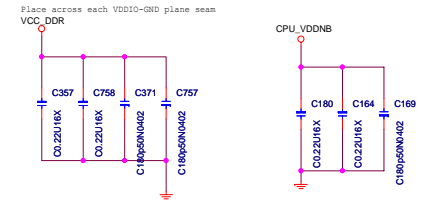


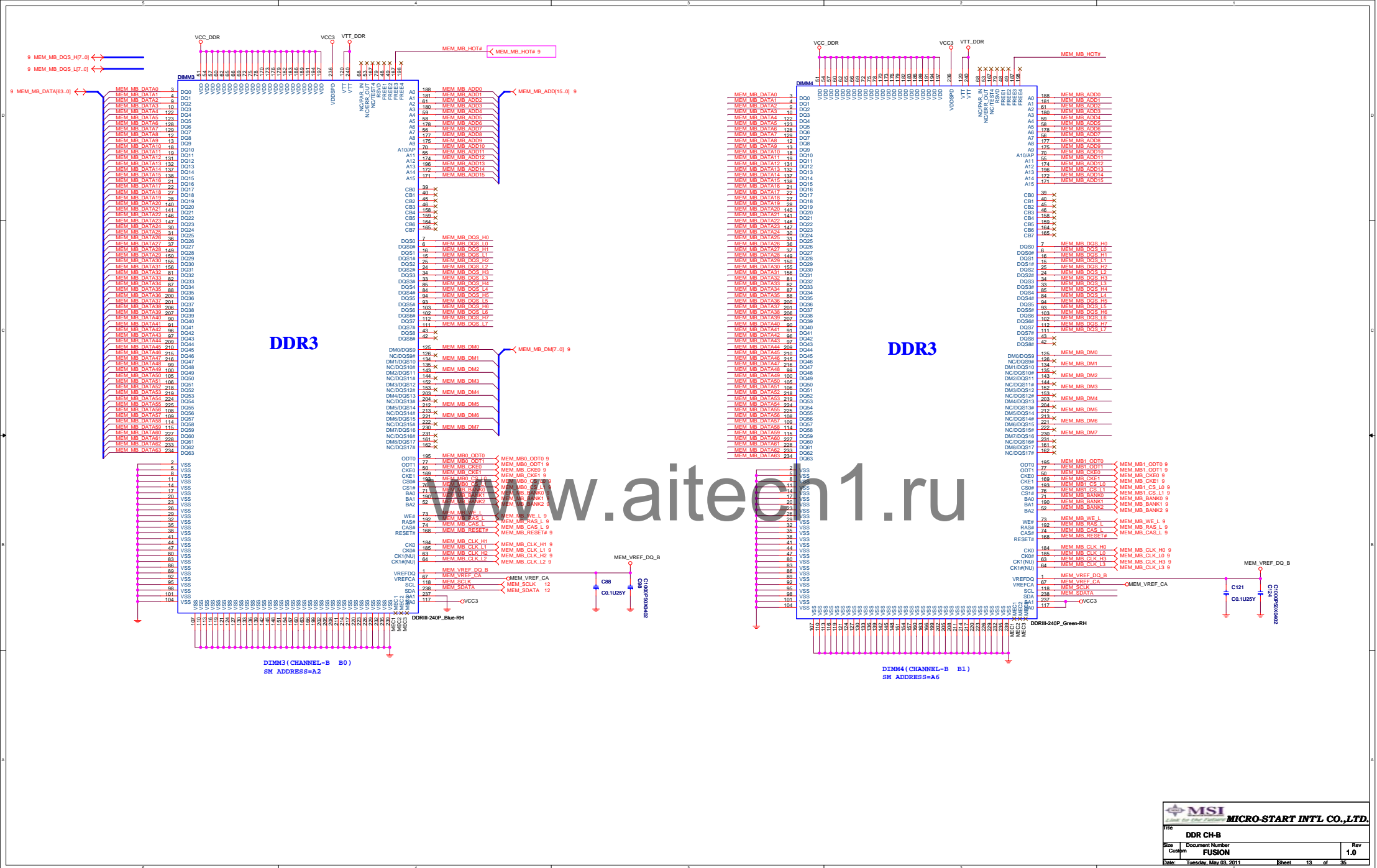
EMC Caps On Bottom side



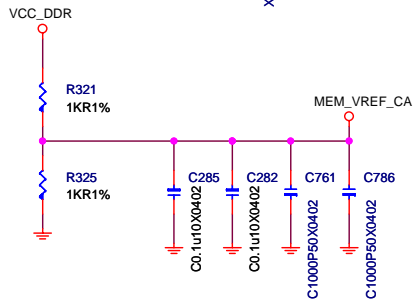
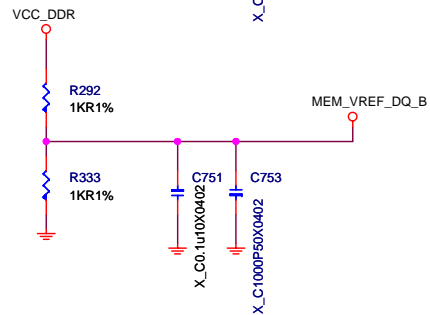
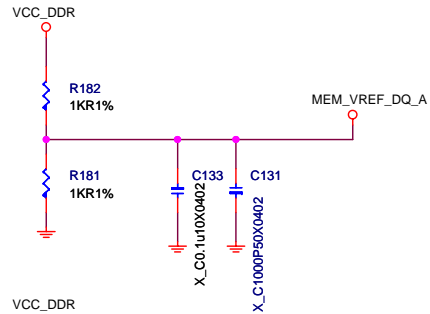
FM1 DECOUPLING CAPS

TOTLE POWER PINS	VSS	VDD	VDDNB	VDDIO	VDDP	VDDR	VDDA	Mref
416	226	102	19	51	8	8	4	2
VALUE/SIZE/ MATERIAL	COMB	COMB	SPLIT	SPLIT	NEAR	FAR		
220/1206/X5R	/	11	2	4	/	/	/	/
100/0805/X5R	/	7	2	1	2+1(B)	1	/	/
4.7U/0805/X5R	/	3	1	4	2	2+2	2	1
0.22U/0603/X5R	/	2	2	2+2	2	2+2	2	1
0.10U/0603/X5R	/	/	/	/	/	/	/	1
0.01U/0603/X5R	/	4	/	/	/	/	/	/
3.3 nF/0603/X5R	/	/	/	/	/	/	/	1
1 nF/0603/X5R	/	/	/	/	/	/	/	1
1 nF/0603/X5R	/	/	/	/	4	/	/	/
180 pF/0603/X5R	/	3	1	2+2	2+2	2	/	/



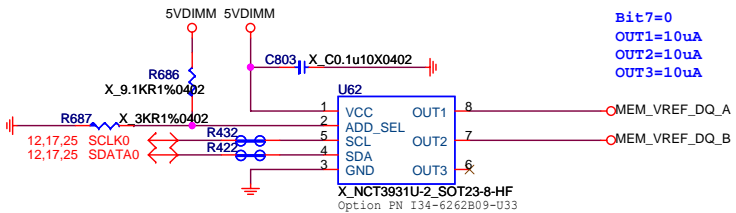


DDR REF POWER & CAPS



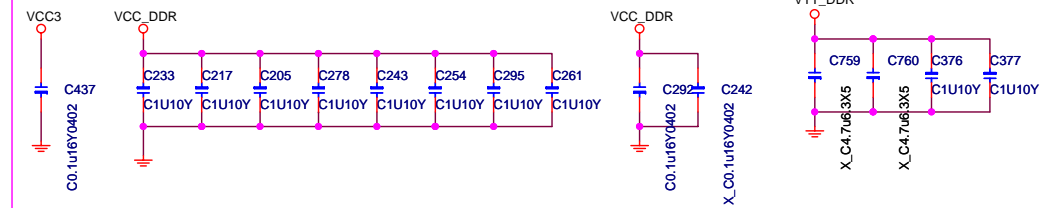
VOLTAGE CONSOLE

0x28:RH=9.1K,RL=3K;Bit7=0




Bit7=0
OUT1=10uA
OUT2=10uA
OUT3=10uA

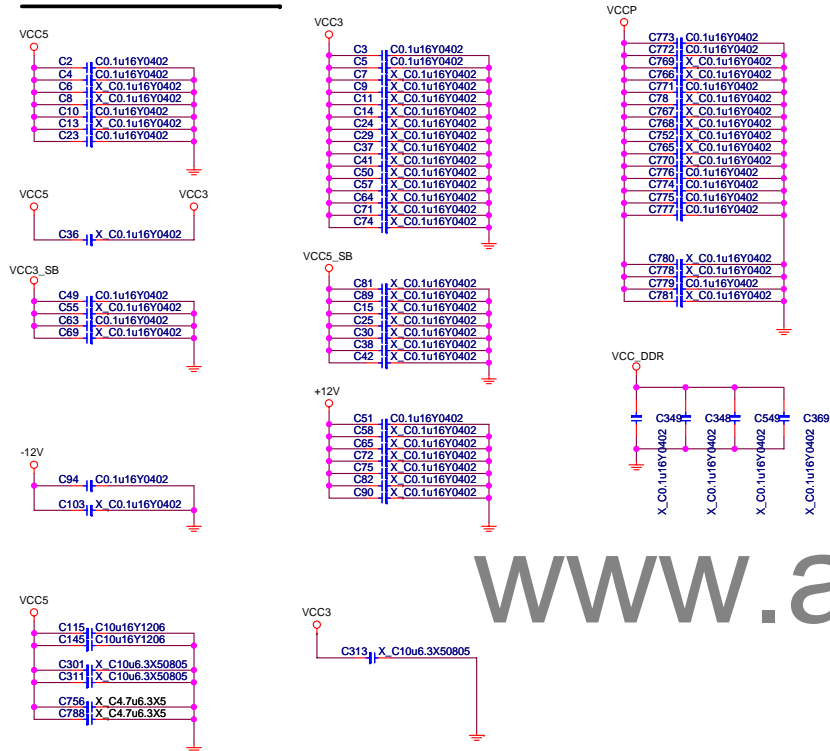
De-coupling Caps For DIMMs



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 MICRO-START INT'L CO.,LTD.		
Title		
DDR REF POWER & CAPS		
Size	Document Number	Rev
B	FUSION	1.0
Date:	Friday, April 29, 2011	Sheet 14 of 35

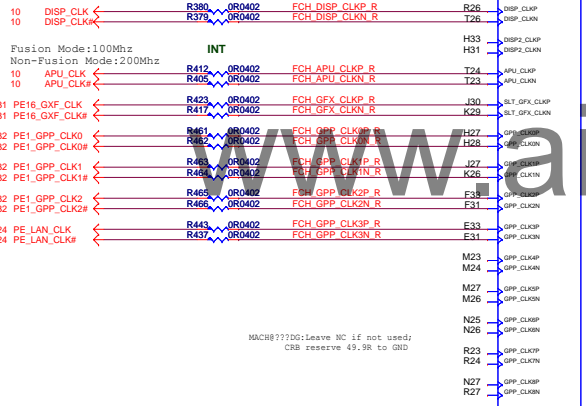
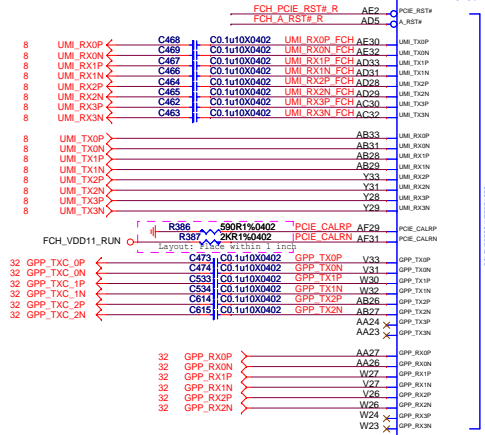
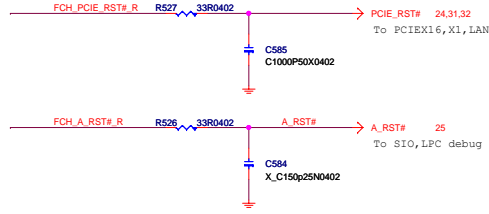
EMI Reserved



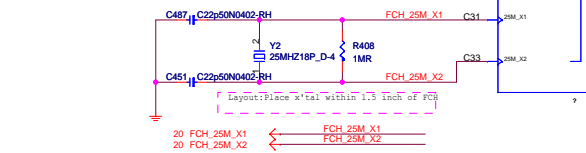
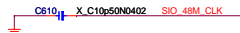
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HUDSON PCIE/PCI/APU/LPC/CLK

A_RST# for LPC device;
PCIE_RST# for APU PCIE device;
PCIE_RST#2 FCH PCIE device



For external clock generator mode:
100-MHz reference clock for the FCH. Spreadcapable.
For internal clock generator mode:
Not used. Left unconnected.
The function is selected by the pin strap "CLKGEN"
(pin LPCCCLK1).



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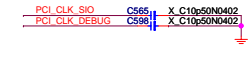
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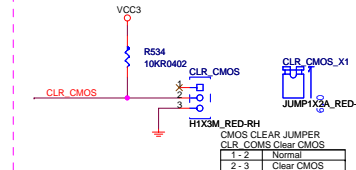
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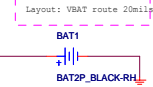


If PCI not implemented: Provide test points
or other means to allow access for debug purposes.
use these balls for alternate GPIO/GPO functions
or leave unconnected.

CLEAR CMOS



Note: LDT_PG, LDT_STP# & LDT_RST# are OD
and require a PU to the APU I/O rail.
They are also in the S5 domain to prevent glitching at
power up.



Layout: Place x'tal within 1.3 inch of FCH

Layout: Place x'tal within 1.3 inch of FCH

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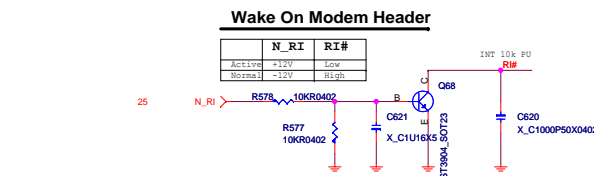
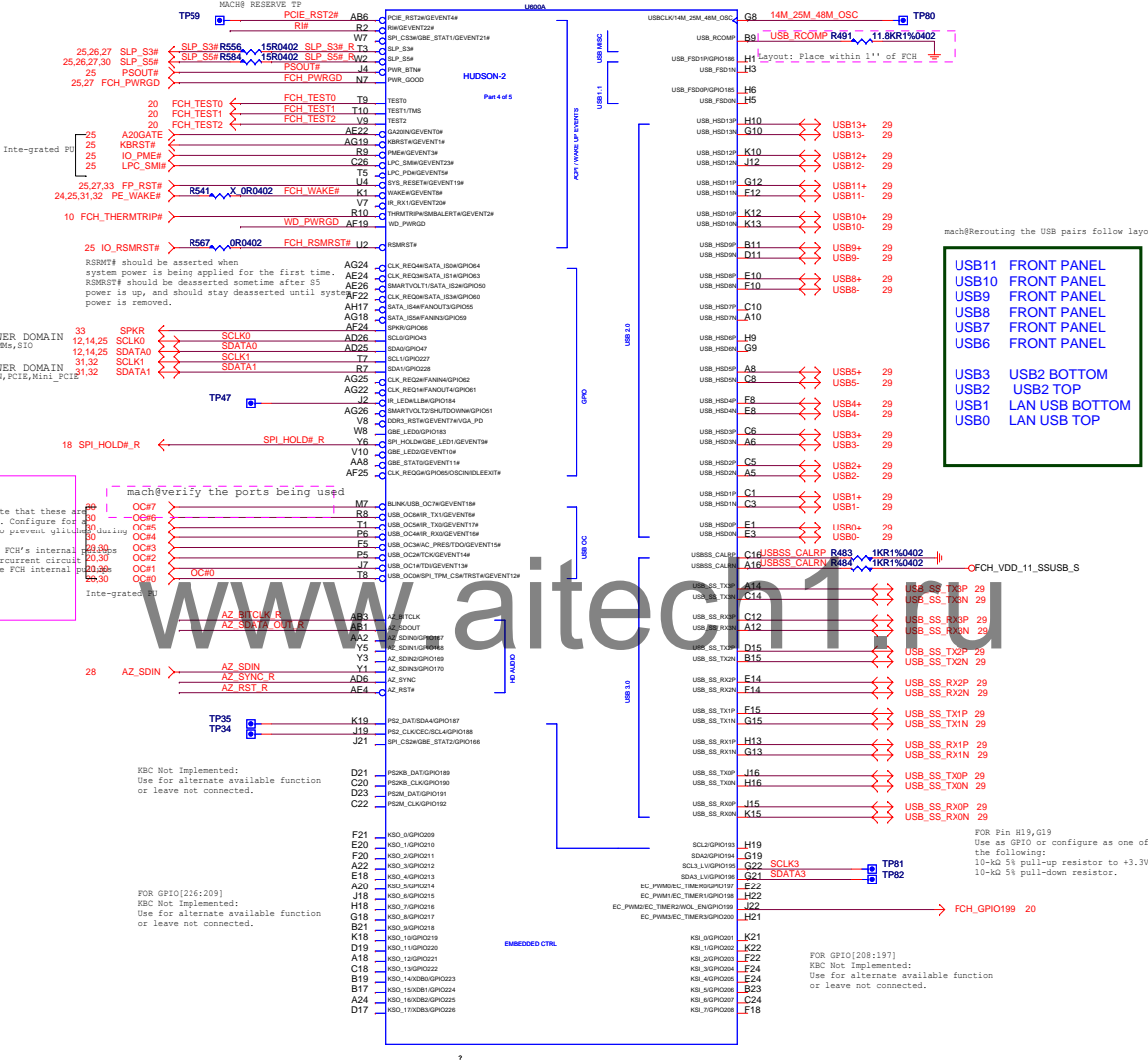
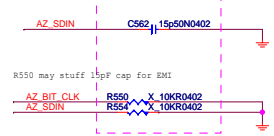
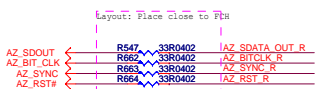
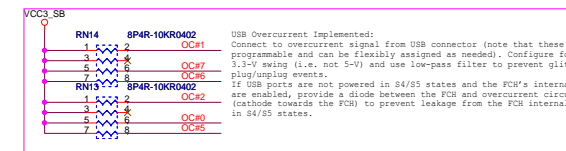
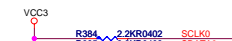
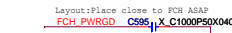
Layout: Place x'tal within 1.3 inch of FCH

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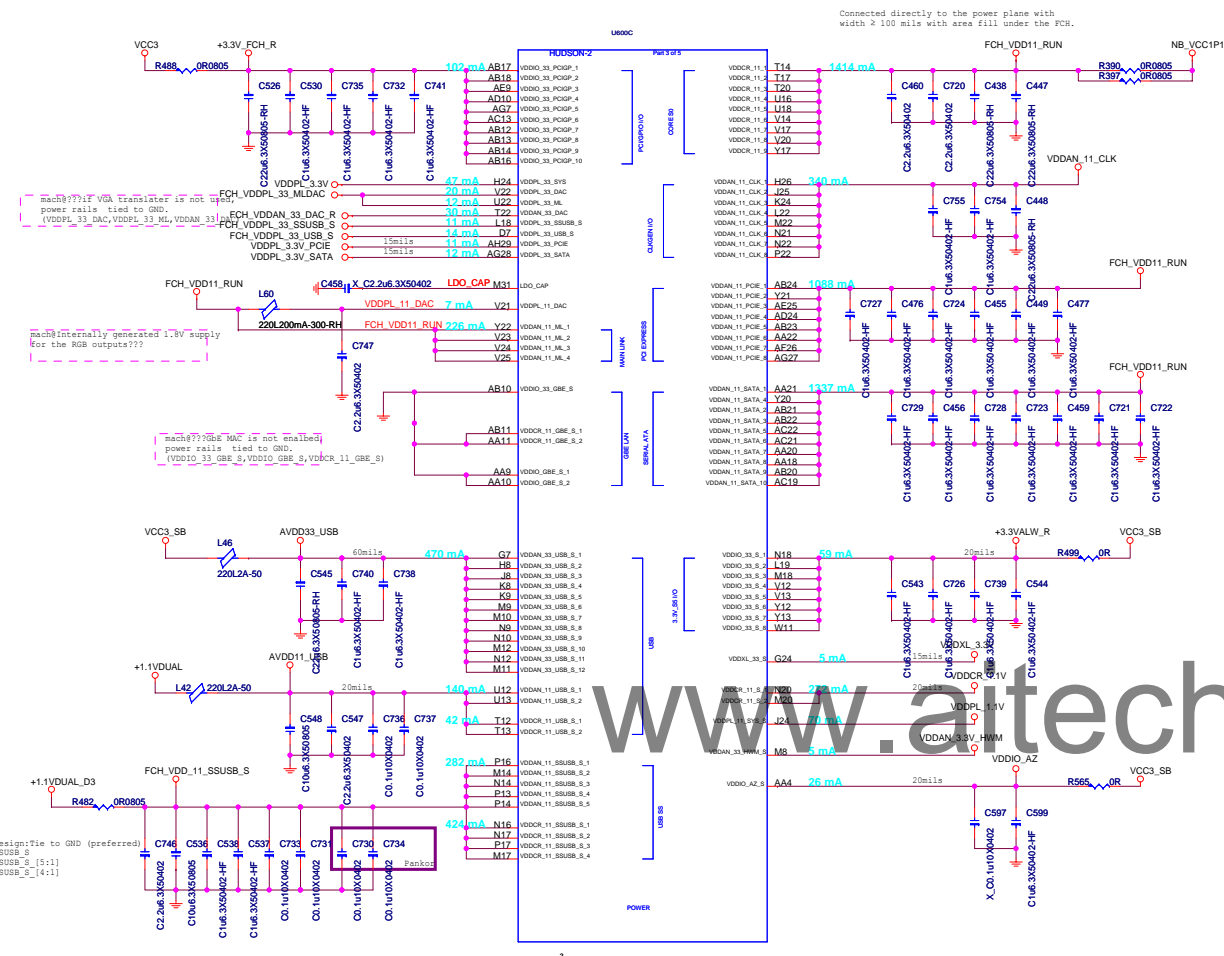
HUDSON ACPI/USB/AZ/GPIO



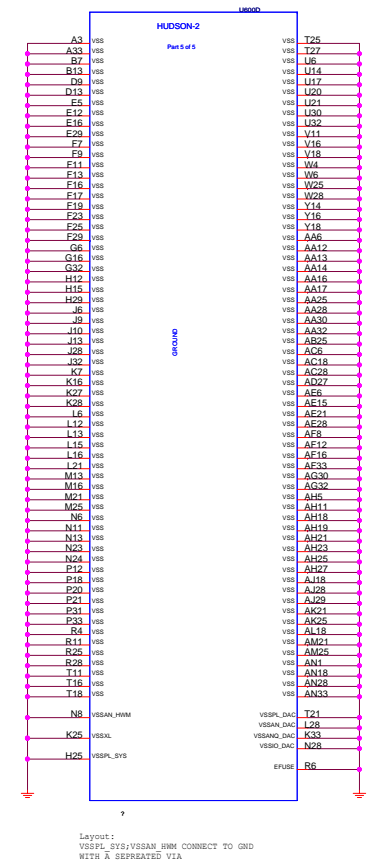
Wake On Modem Header

	N_RI	RI#
Active	+12V	Low
Normal	-12V	High

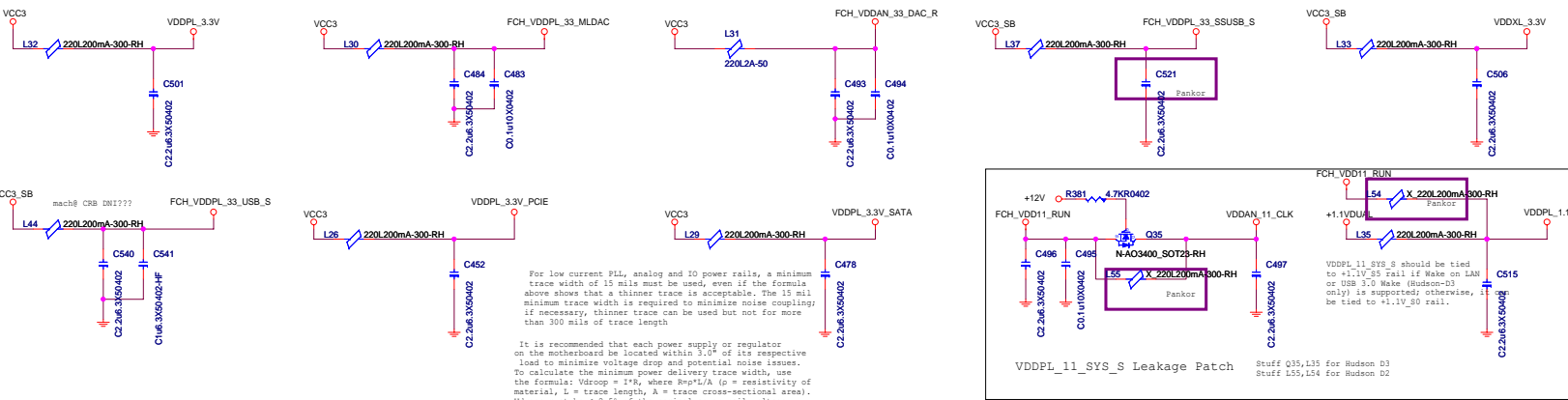
HUDSON POWER&DECOUPLING



Power Rails	Hudson D3	Hudson D2
NB_VCC1P1	max	4412 mA
VDDCR_11_[9:1]	1120 mA	1414 mA
VDDAN_11_CLK_[8:1]	340 mA	
VDDAN_11_FCIE_[8:1]	1088 mA	
VDDAN_11_SATA_[10:1]	1337 mA	
VDDAN_11_ML_[4:1]	226 mA	
VDDFL_11_DAC	7 mA	
VCC3	max	319 mA
VDDIO_33_PCFGIP_[10:1]	102 mA	
VDDPL_33_SYS	47 mA	
VDDPL_33_DAC	20 mA	
VDDPL_33_ML	12 mA	
VDDPL_33_FCIE	11 mA	
VDDPL_33_SATA	12 mA	
VDDAN_33_DAC	30 mA	
VCC3_SB	max	659 mA
VDDIO_33_S_[8:1]	59 mA	
VDDIO_A2_S	26 mA	
VDDXL_33_S	5 mA	
VDDAN_33_HWM_S	12 mA	
VDDIO_GBE_S[2:1]	145 mA	GND
VDDIO_33_GBE_S	2 mA	GND
VDDPL_33_USB_S	14 mA	
VDDAN_33_USB_S_[12:1]	470 mA	
VDDPL_33_SSUSB_S	11 mA	0 mA
+1.1VPUAL	max	1293 mA
VDDCR_11_S_[2:1]	272 mA	
VDDCR_11_GBE_S[2:1]	63 mA	GND
VDDPL_11_SYS_S	70 mA	
VDDAN_11_USB_S_[2:1]	140 mA	
VDDCR_11_USB_S_[2:1]	42 mA	
VDDAN_11_SSUSB_S	5282 mA	0 mA
VDDCR_11_SSUSB_S_[4:2]	428 mA	0 mA

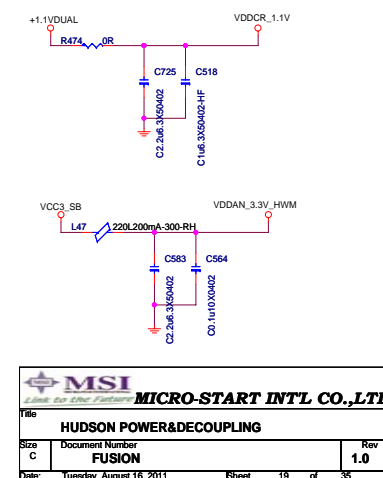


LAYOUT:
ROUTE THE POWER TRACES 15MILS WIDTH AT LEAST
PLACE THE DECOUPING CAPS CLOSE TO FCH ASAP
PLACE FB<=1" ,CAPS <=0.2"

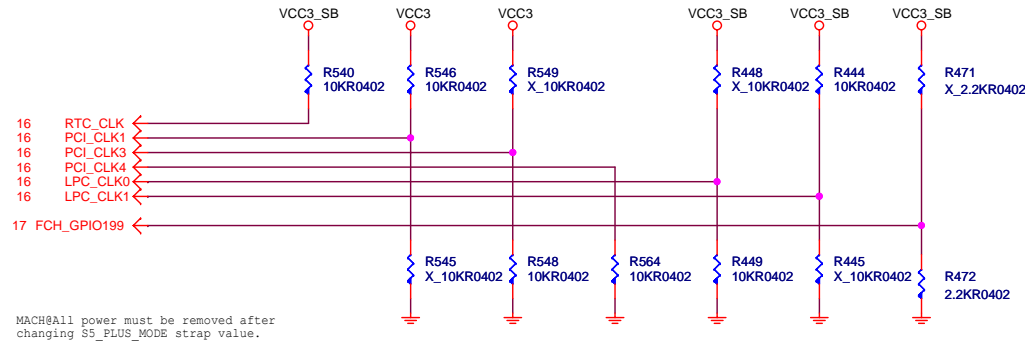


For low current PLL, analog and 10, power rails, a minimum trace width of 15 mils must be used, even if the formula above shows that a thinner trace is acceptable. The 15 mil minimum trace width is required to minimize noise coupling. If necessary, thinner trace can be used but not for more than 300 mils of trace length.

It is recommended that each power supply or regulator on the motherboard be located within 3.0" of its respective decoupling capacitor and potential noise issues. To calculate the minimum power delivery trace width, use the formula: $W(\mu\text{m}) = I \cdot R$, where $R = \rho \cdot L / A$ (ρ = resistivity of material, L = trace length, A = trace cross-sectional area). I = current, R = resistance, ρ = resistivity, L = distance from power source to terminal power rail voltage under maximum current conditions.



FCH REQUIRED STRAPS



	RTCCLK	PCI_CLK1	PCI_CLK3	PCI_CLK4	LPC_CLK0	LPC_CLK1	GPIO199
PULL HIGH	S5 PLUS MODE DISABLED DEFAULT	ALLOW PCIE GEN2 DEFAULT	USE DEBUG STRAPS	Reserved	EC ENABLED	INTERNAL CLOCK GEN ENABLED DEFAULT	LPC ROM
PULL LOW	S5 PLUS MODE ENABLED	FORCE PCIE GEN1	IGNORE DEBUG STRAPS DEFAULT	Required setting for intergrated CLOCK MODE DEFAULT	EC DISABLED DEFAULT	INTERNAL CLOCK GEN DISABLED	SPI ROM DEFAULT

FCH DEBUG STRAPS

Provided test point access for lab use.
FCH HAS 15K INTERNAL PU FOR PCI_AD[27:23]

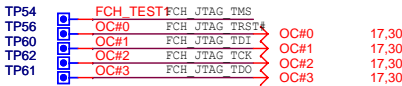


	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	USE PCI PLL DEFAULT	RESERVED	Normal REFCLK Termination DEFAULT	USE DEFAULT PCIE STRAPS DEFAULT	DISABLE PCI MEM BOOT DEFAULT
PULL DOWN	BYPASS PCI PLL	RESERVED	Inverted REFCLK Termination	USE EEPROM PCIE STRAPS	ENABLE PCI MEM BOOT

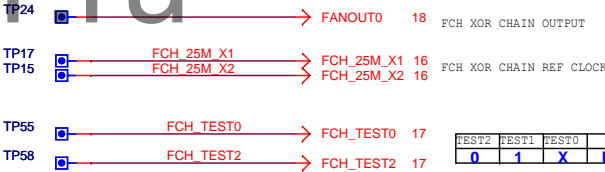
FCH PCIE EEPROM STRAPS



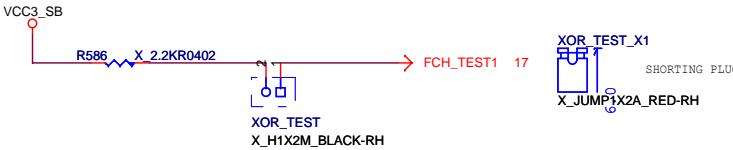
FCH ICE DEBUG /JTAG TEST PINS




FCH XOR CHAIN TEST



TEST2	TEST1	TEST0	Description
0	1	X	Enable test mode





MICRO-START INT'L CO.,LTD.

Title

HUDSON STRAPS

Size B

Document Number

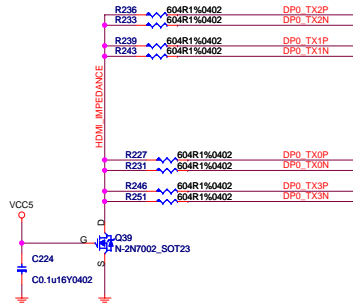
FUSION

Date: Friday, April 29, 2011

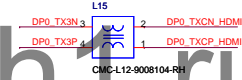
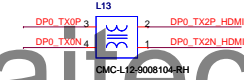
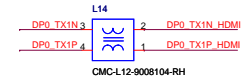
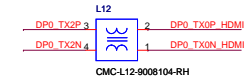
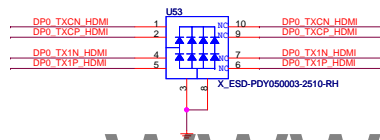
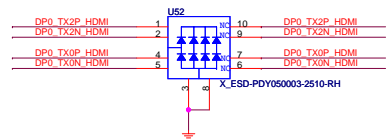
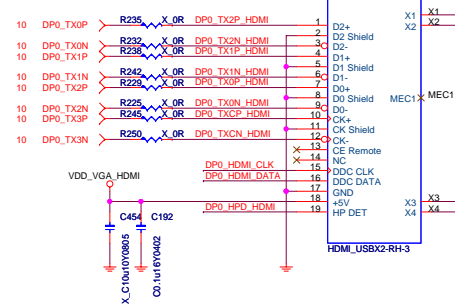
Sheet 20 of 35

Rev 1.0

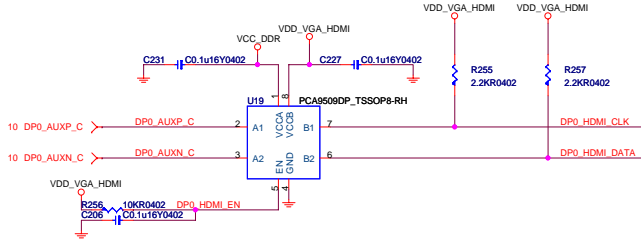
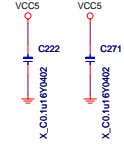
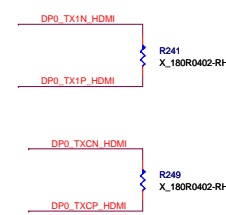
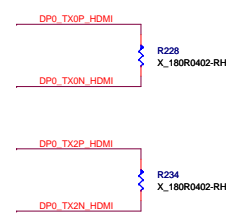
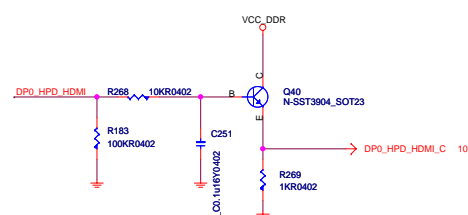
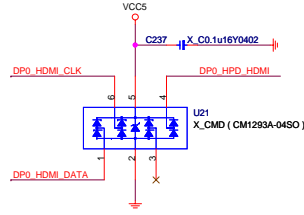
HDMI CONN,

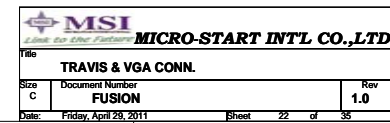


DP CONFIGURATION TABLE					
INTERFACE	DP PORT OF PM1				
DP	3	2	1	0	
HDMI	Channel1Clock	Ch 0	Ch 1	Ch 2	



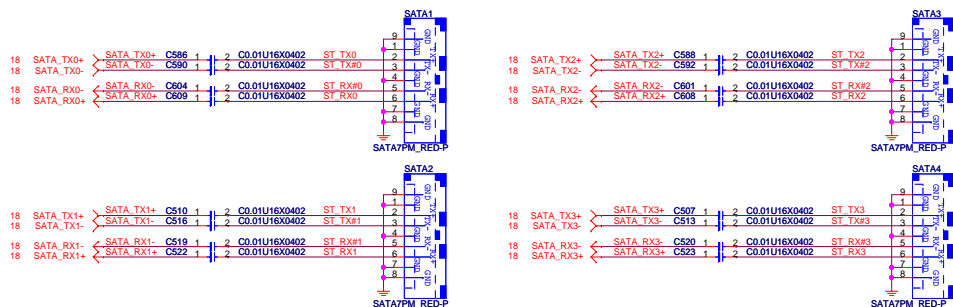
www.aitech1.ru

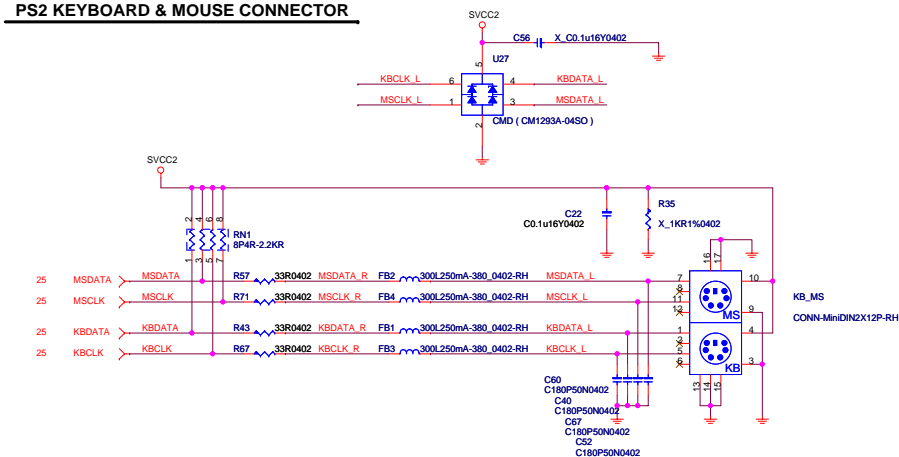




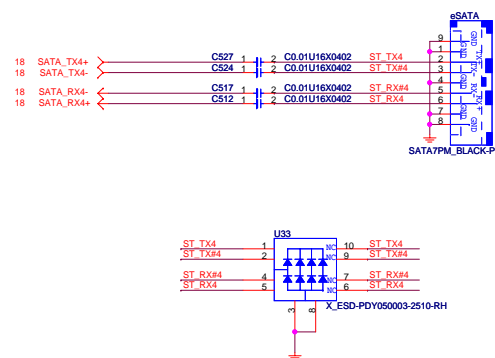
Multiple eSATA function

Layout: For Gen 3.0, trace length within 3''

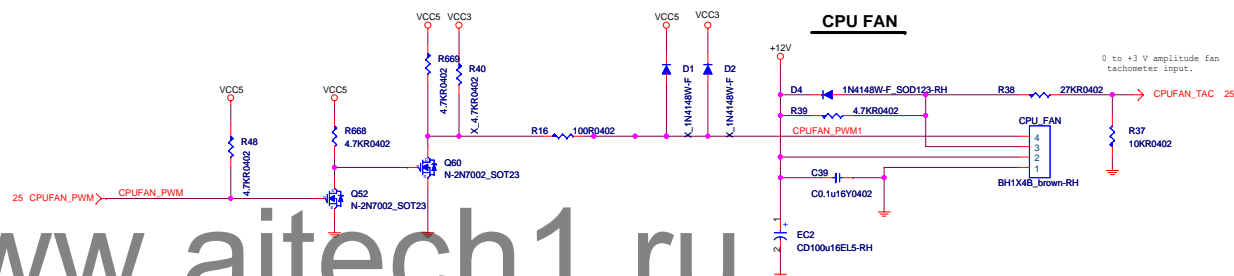


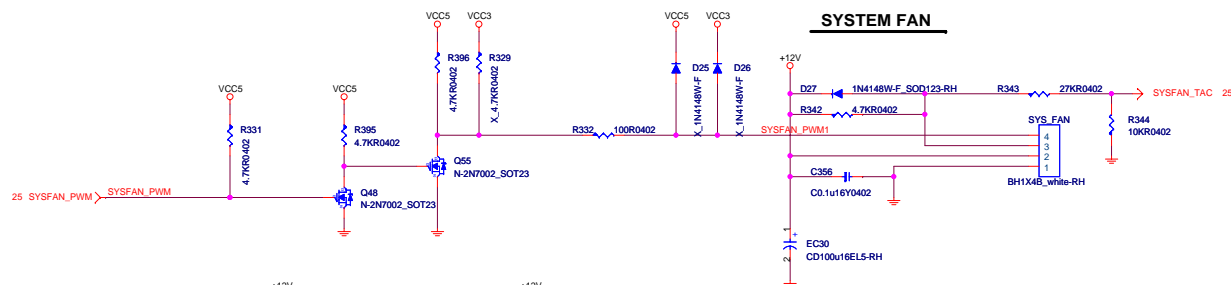


Layout: For onboard eSATA conn. without redriver IC, trace length within 6"

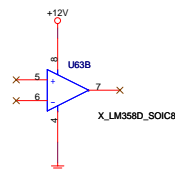
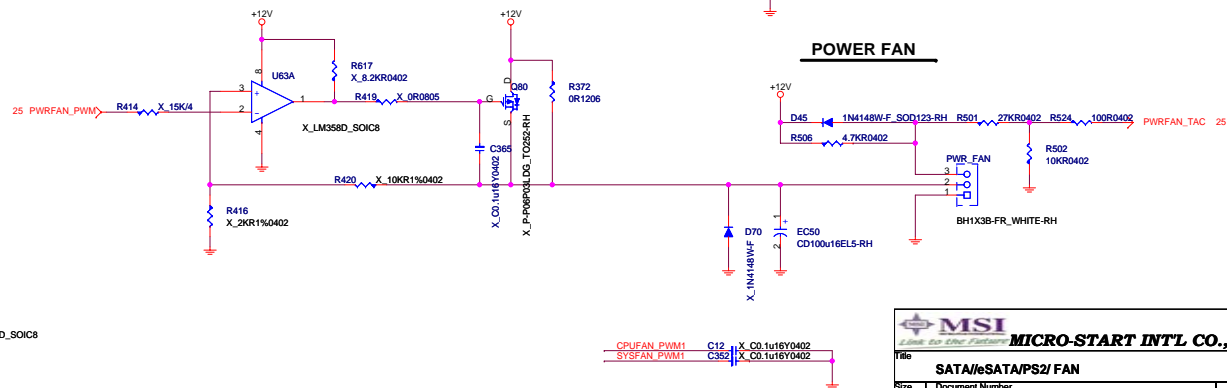


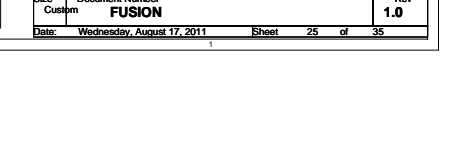
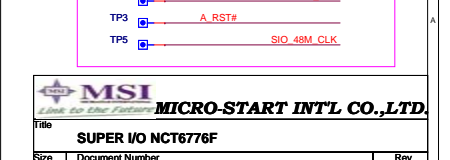
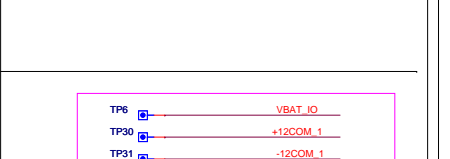
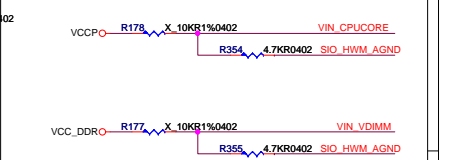
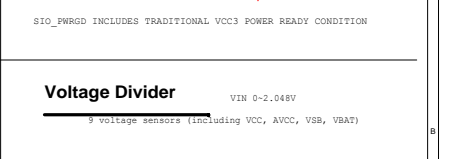
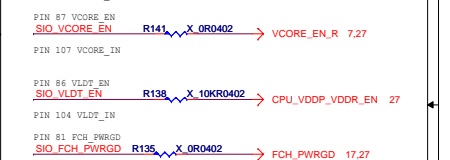
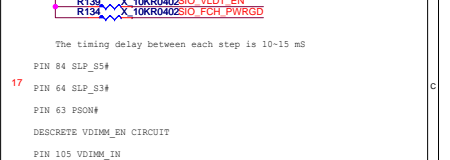
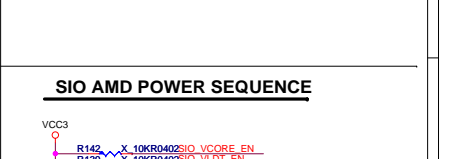
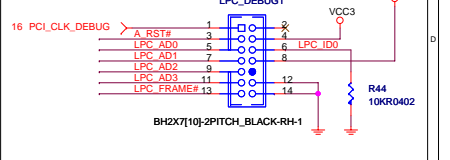
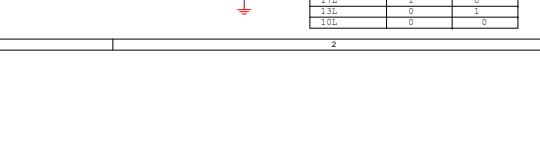
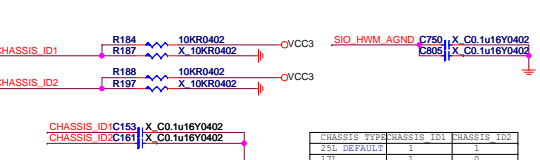
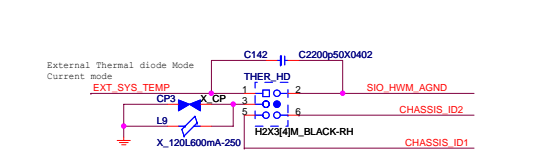
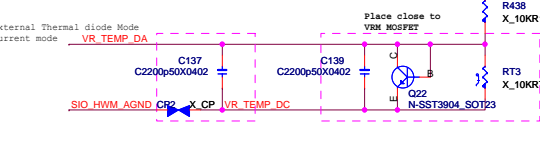
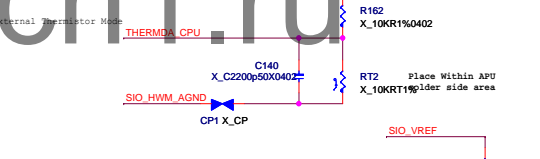
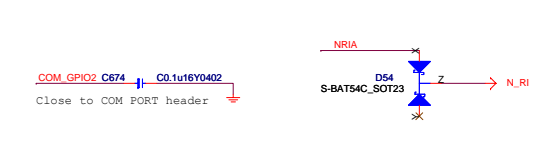
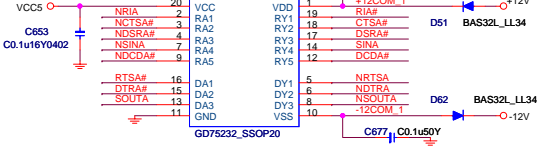
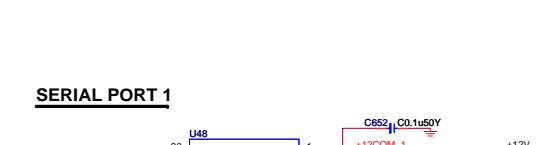
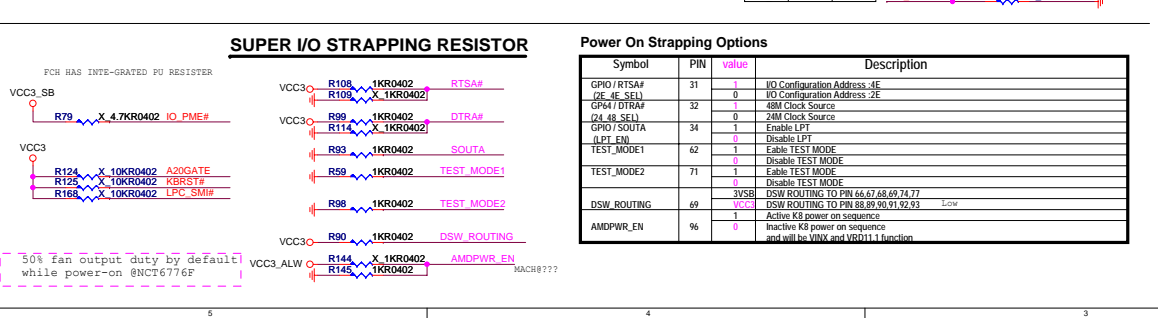
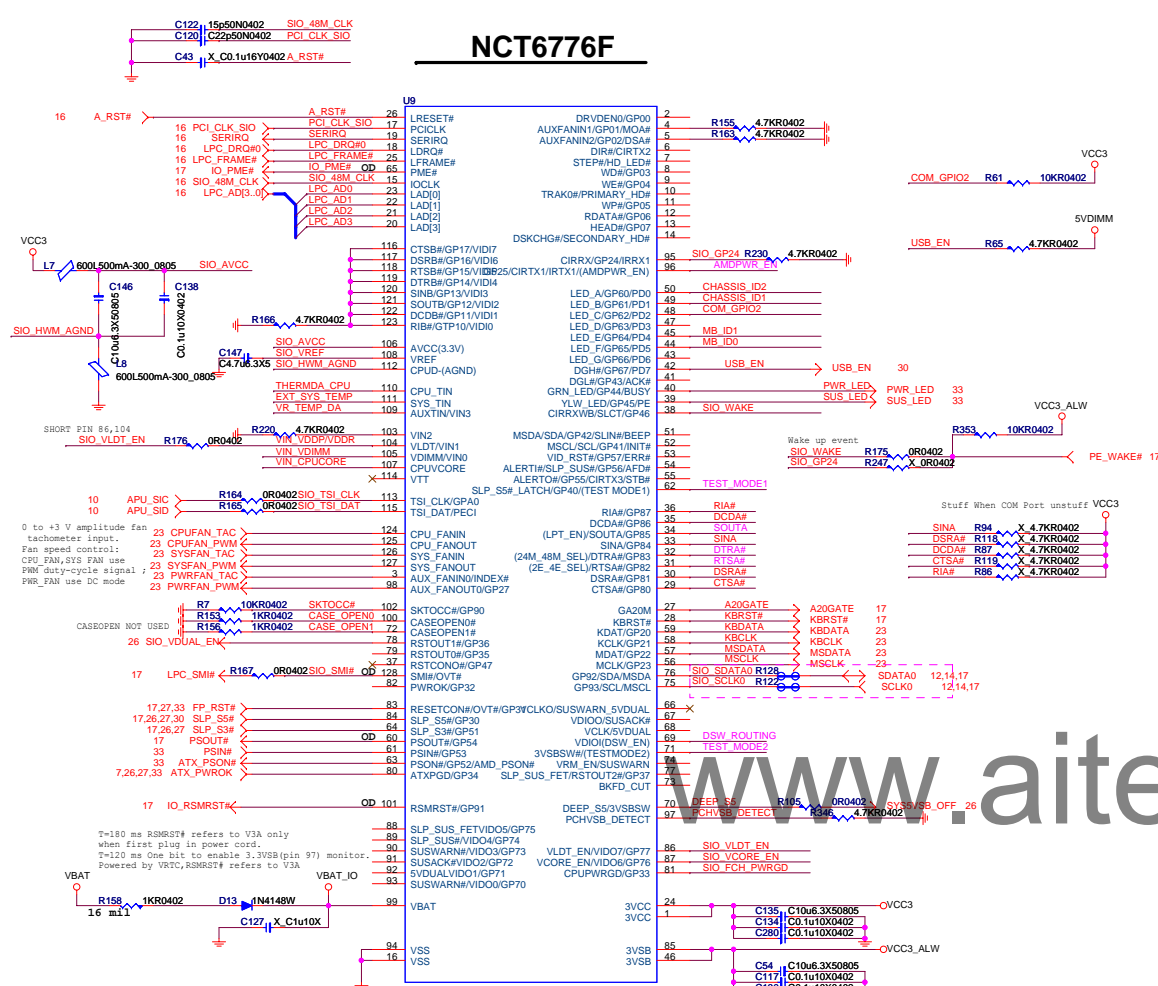
UNIT 11: THE FUTURE



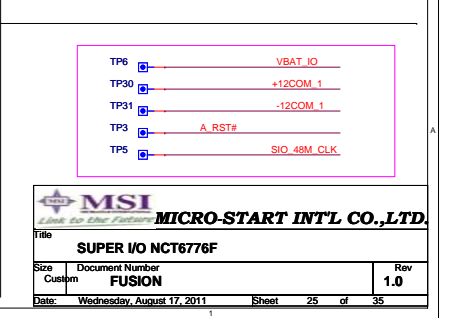
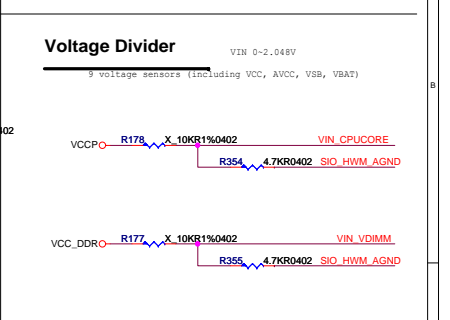
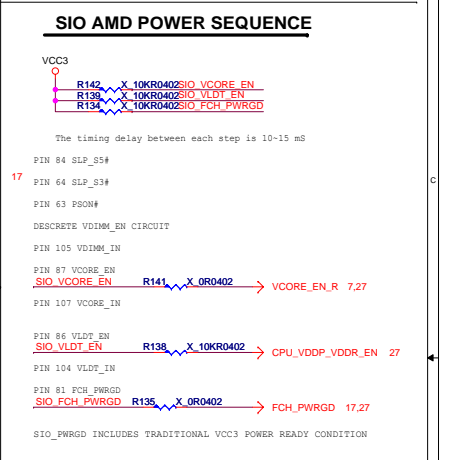
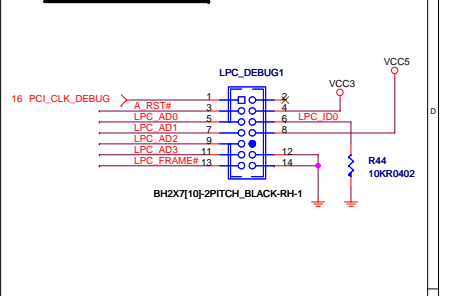


CONCLUSION

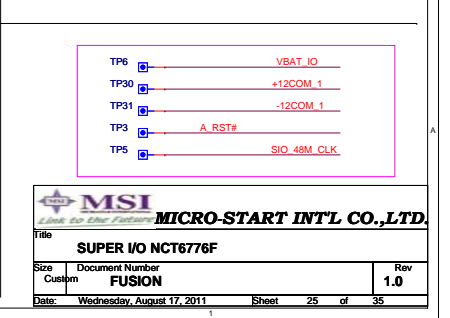
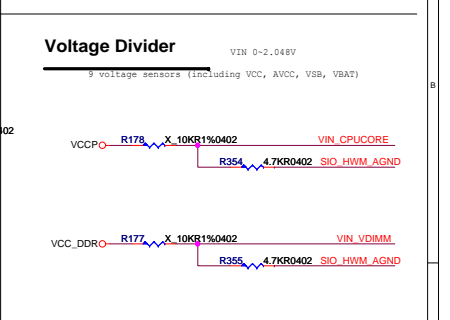
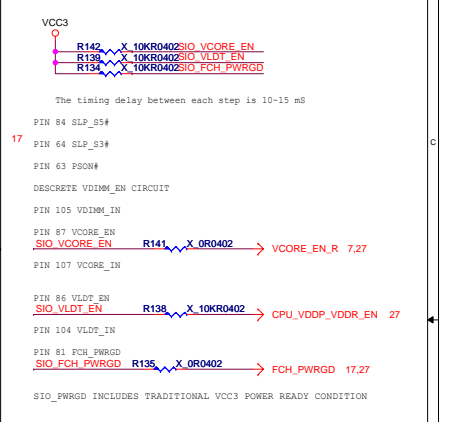




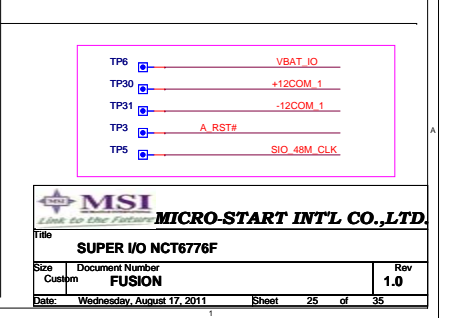
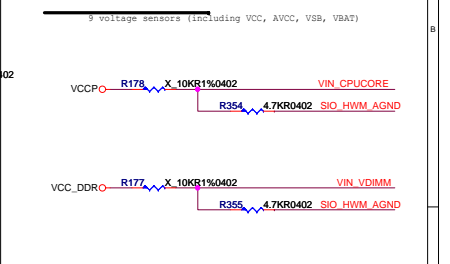
LPC Debug



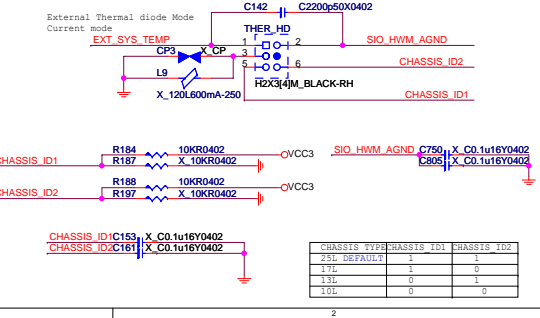
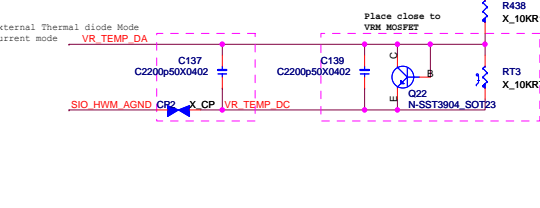
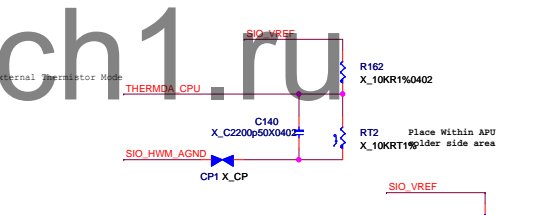
SIO AMD POWER SEQUENCE



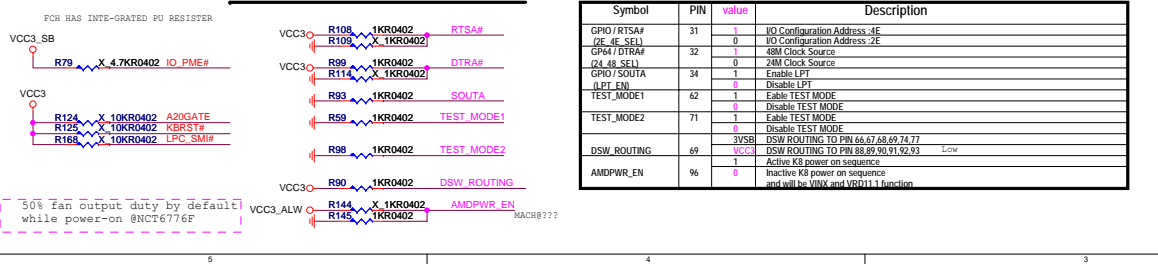
Voltage Divider



TEMP SENSOR



SUPER I/O STRAPPING RESISTOR



Power On Strapping Options

Symbol	Pin	Value	Description
GPO/RTSA#	31	1	IO Configuration Address -4E
DE_4E_SEL	32	0	IO Configuration Address -2E
GP4/DTRA#	33	0	48M Clock Source
D4_48_SEL	34	0	24M Clock Source
GPO/SOUTA	35	1	Enable LPT
LPT_EN	36	0	Disable LPT
TEST_MODE1	62	1	Enable TEST MODE
TEST_MODE2	71	1	Enable TEST MODE
DSW_ROUTING	69	3VSB	DSW ROUTING TO PIN 66,67,68,69,74,77
AMDPWR_EN	96	1	Active K8 power on sequence
			Inactive K8 power on sequence and will be VDD and VDD011 function



MICRO-START INTL CO.,LTD

SUPER I/O NCT6776F

Size: 25L DEFAULT 1 0
Custom: 13L 1 0
10L 0 1

Rev: 1.0

Date: Wednesday, August 17, 2011 Sheet: 25 of 35

VCC5_SB Power Switch

SO,S1,S3

Trace Width 80mils.

Tune 5VSB Inrush current to 2A from 4A

ATX_5VSB

Option for Normal State

VCC5_SB

Layout: Place close to
UF7706 pin3 A3A

EC59
CD1000U6.3EL11.5

R552 X OR L206
R553 X OR L206

G62
S
P-P06P03LCO_SOT89-3-RH

R514
249K01%

EC54
CD10u10EL5

R531
10K0R005

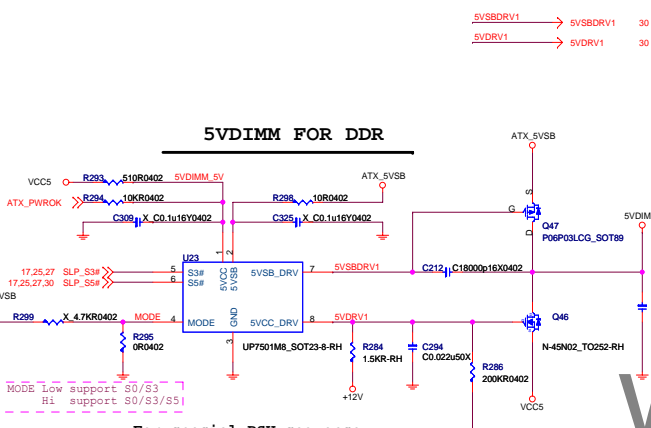
C566
C1U16ES

EC67: Prevent 5VSB vibration
if there is no vibration on VCC5_SB,
place EC67 at ATX_5VSB side

EC75 prevent ATX_5VSB
inrush current over 2A

High-----Q20 OFF
Low-----Q20 ON

25 SYSVSB_OFF



CPU VDDA_25 POWER

Layout:Route 50 mils AND 500 mils LONG
(USE 2x15 mil TRACKS TO EXIT BALL FIELD)

3 ATX_PWROK

VCC3

VCC5_SB

R557 10R

C782 X.C0.1u16V0402

R362 10K0402

VCC3

C389 C10uV0405

C390 X.C0.1u16V0402

U54 LP1010PSW8_PSOP8+HF

2.5V@0.75 A

VDDA_25

EC29 CD10

C373 X.C0.1u16V0402

R361 2.1KR1%0402 R2

C374 X.C0.1uV0405

0.8 V

R356 1KR1%0402 R1

Pin1: 9 M

Vo=0.8* (R1+R2) /R1

$P_d = (V_{in} - V_{out}) * I_{max} = (3.3 - 2.5) V * 0.75Amp = 0.6 W$

[illegible][illegible]

The diagram shows a 1.1V LDO regulator circuit. The input is connected to VCC3_SB through a 10R resistor (R500). The input pin (VIN) is connected to VCC3_SB_POK. The feedback pin (FB) is connected to the output through a 10R resistor (R492). The output pin (VOUT) is connected to the output node, which is also connected to a 0.015uF capacitor (C505) to ground. The output voltage is 1.1V. The circuit is powered by VCC3_SB and VCC3_SB_POK. The output is connected to EC66 and X_CD100u16BLS3RH.

For option

ATX_5VSB

VCC3_ALW

U37
U1011/AMAS-00_S0723-5HF

VIN VOUT

EN GND FB

C558 C555

C100nF00805 C0.1uF0V0402

0.8 V

C566 C0.1uF0V0402

R512 3.16K1R100402 R2

C568 C100nF00805

C569 C100nF00805

R513 1K1R100402 R1

VCC3_ALW

$$Pd = (V_{in} - V_{out}) \times I_{max} = (5 - 2.5) V \times 0.2 A_{mp} = 0.5 W$$

$$V_{out} = 0.8 \times (R1 + R2) / R1$$

0.75V@2A

VTT_DDR

VCC_DDR

VCC5

C350 100nF

R327 100k

R328 10k

R329 10k

R330 10k

R331 10k

R332 10k

U26

OP0109PSW8_PS08-PF

VIN

GND

REFIN

VCONT

NC1

NC3

NC2

VOUT

GND

1

2

3

4

5

6

7

8

9

10

11

12

13

14

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410

411

412

4

DUAL POWER CONTROL

ATX_5VSB

R629
X_4.7KOR402

R623
20K R1%Q402

VDUAL_EN
VDUAL_EN=H#AND
(SYSVSB_OFF, SIO_VDUAL_EN)

N:85
L:80,S1,S3

25 SYSVSB_OFF

Q76
N-2N7002_SOT23

C640

X_C0.1u16V0402

SIO GPIO
L:VCC3_WAKE on# 85
N:VCC3_WAKE off#85

25 SIO_VDUAL_EN

R382
4.7KOR402

Q36
NS8T3904_SOT23

R665
X_OR40402

SIO_VDUAL_EN
SYSVSB_OFF

R670
X_OR40402

R411
X_4.7KOR402

R630
X_4.7KOR402

U64
VCC
INB
INA
GND OUTV

VCC3

R849
X_4.7KOR402

VCC3

R671
X_OR40402

VDUAL_EN

X_TC79H400FV_SSOP5-RH

VCC5

EC19
CD1000U3.3EL11.5

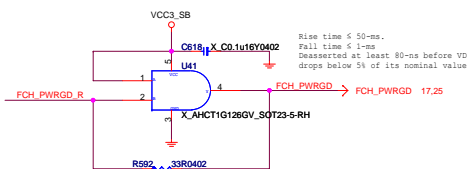
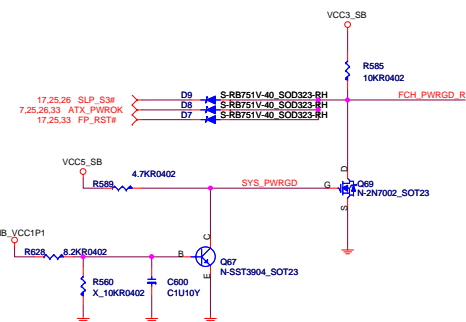
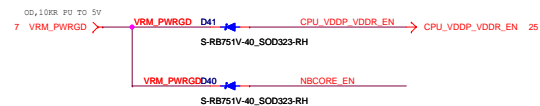
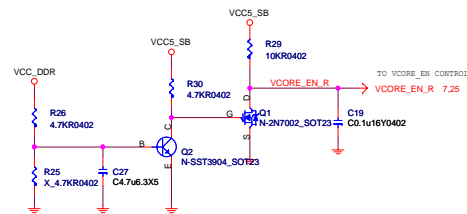
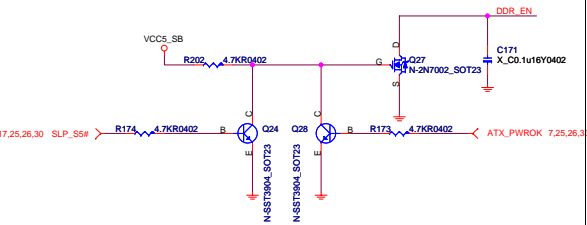
EC65
CD1000U3.3EL11.5

VCC3

EC43
CD1000U3.3EL11.5

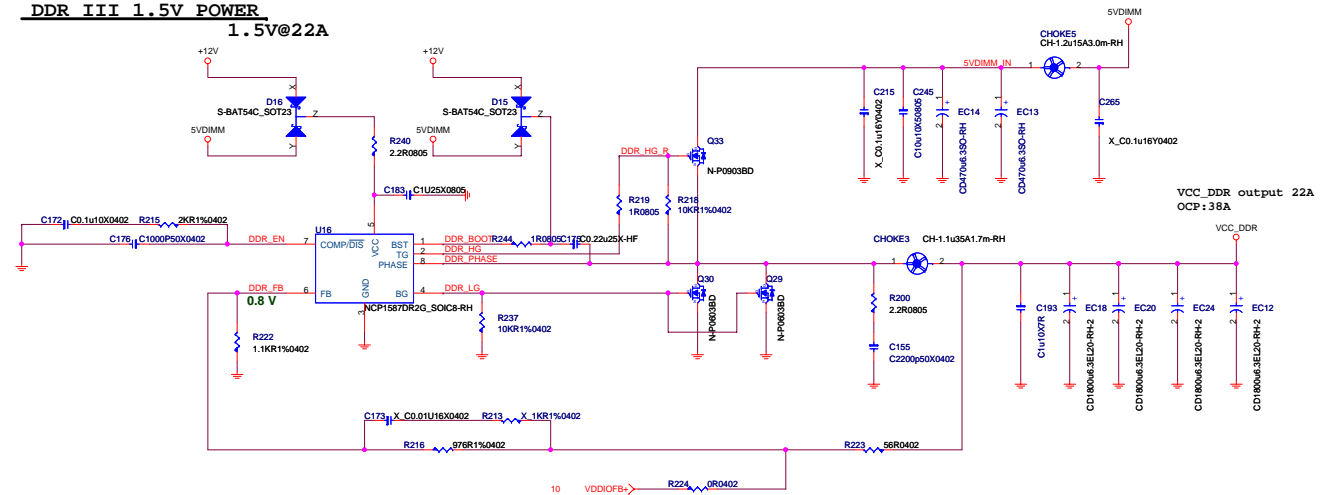
EC45
CD1000U3.3EL11.5

POWER EN & PWRGD LOGIC CIRCUIT



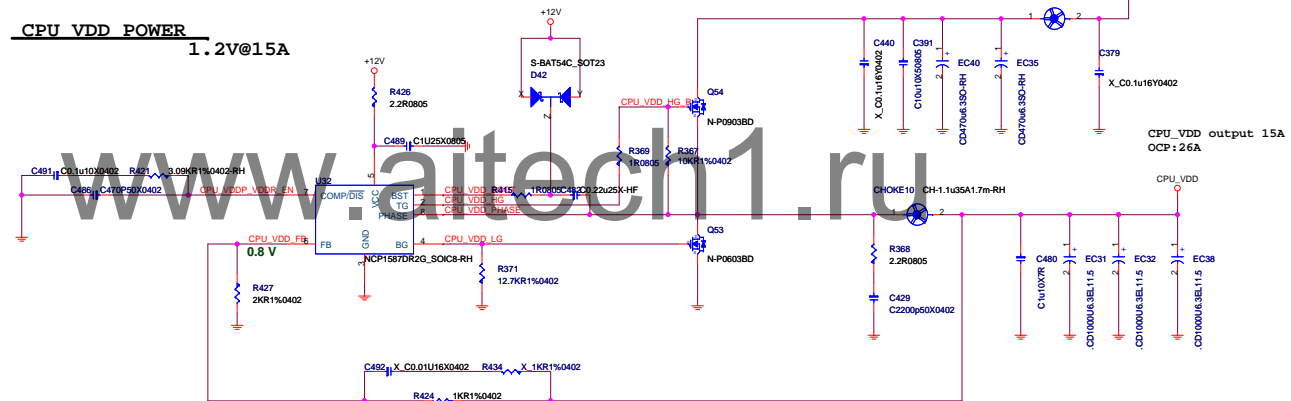
DDR III 1.5V POWER

1.5V@22A



CPU VDD POWER

1.2V@15A



VDDP and VDDR support two separate power planes with single regulator

CPU_VDDP POWER 1.2 V@5A

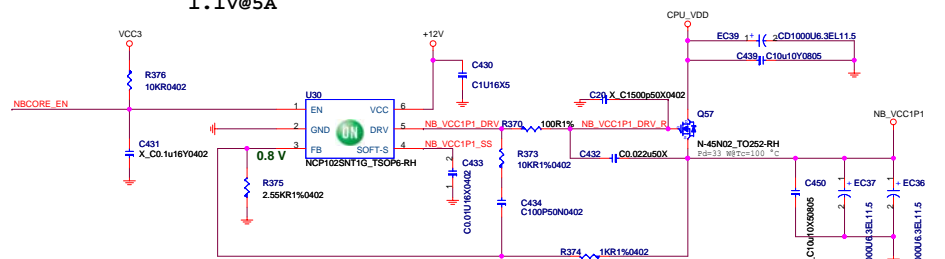


CPU_VDDR POWER 1.2 V@5A



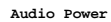
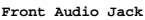
NB VCC1P1 POWER

1.1V@5A



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FCH CORE & DDR Power			
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Default is ALC892



Reference resistor for Jack Detection (close to the codec)

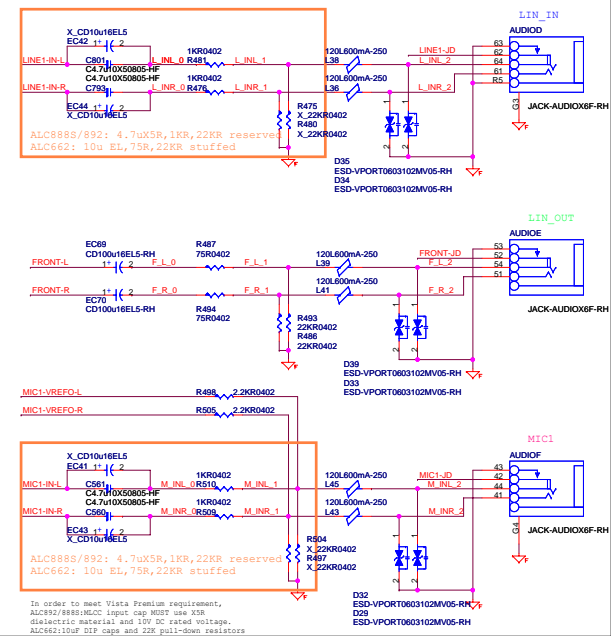
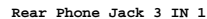
Split by DGND

Analog Area

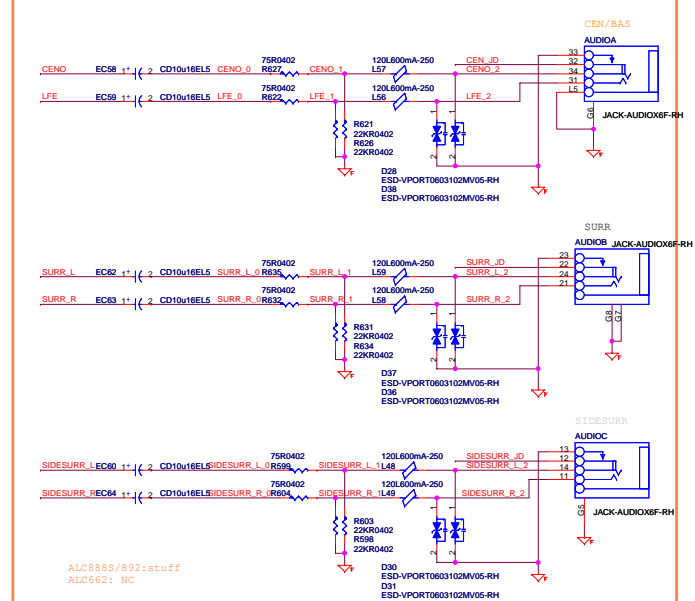
Digital Area

The diagram shows a microcontroller pinout with the following connections:

- Reference resistor for Jack Detection (close to the codec):** A blue line connects PIN.38 to PIN.23.
- Split by DGND:** A red line connects PIN.66 to PIN.13.
- Analog Area:** A blue line connects PIN.37 to PIN.24.
- Digital Area:** A blue line connects PIN.41 to PIN.12.
- Other pins shown:** PIN.38, PIN.23, PIN.37, PIN.24, PIN.66, PIN.41, PIN.40, PIN.13, PIN.1, PIN.12.



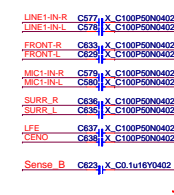
Rear Phone Jack 6 IN 1



EMI

For ENI

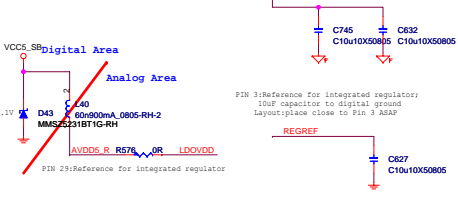
Placement close to Codec chip



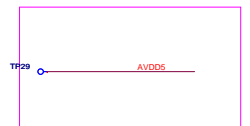
ALC892 PART

ALC662-VC/88S:NC
#10000/662 MB=10000/662

ALC892/662-VD:stuff



	ALC892	ALC888S-VC	ALC662-VC	ALC662-
AVDD(5V)	45.8mA	61mA	41.5mA	40.5mA
DVDD(3.3V)	11mA	41mA	23.4mA	10.8mA



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ALC892/662			
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NEAR USB CONNECTOR

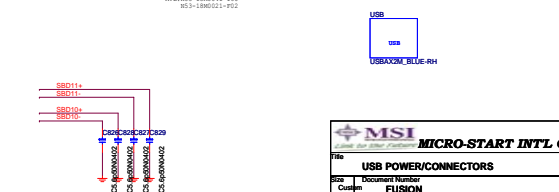
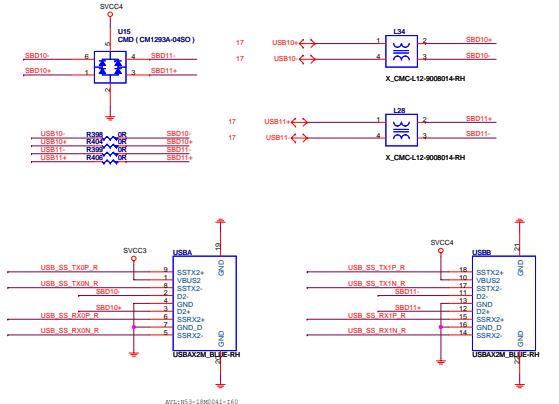
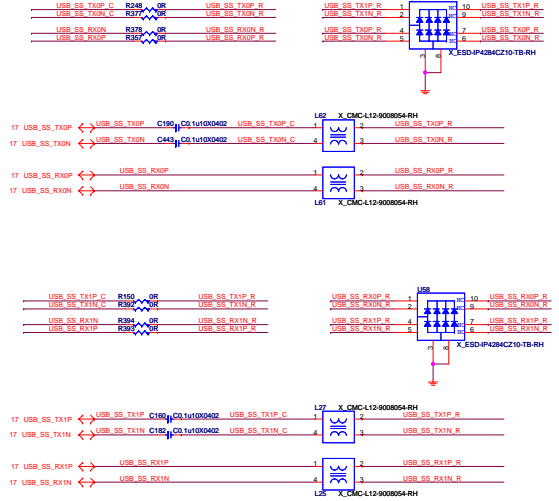
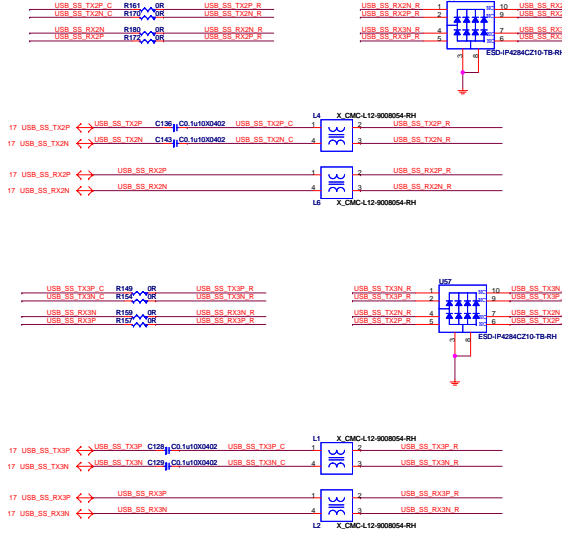
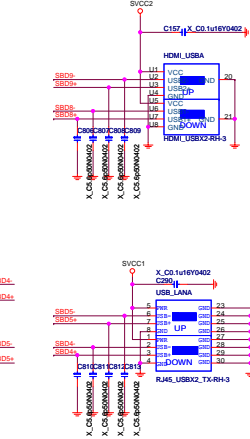
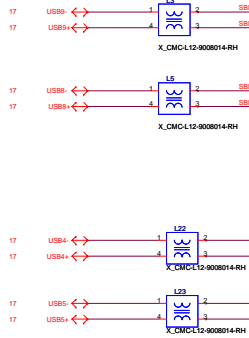
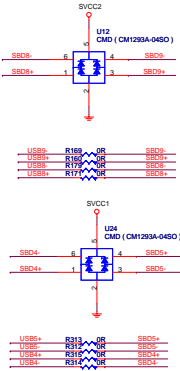
REAR PANEL USB CONNECTOR

FRONT USB PIN HEADER

USB 2.0 trace length
REAR side within 18'';
FRONT side within 6''

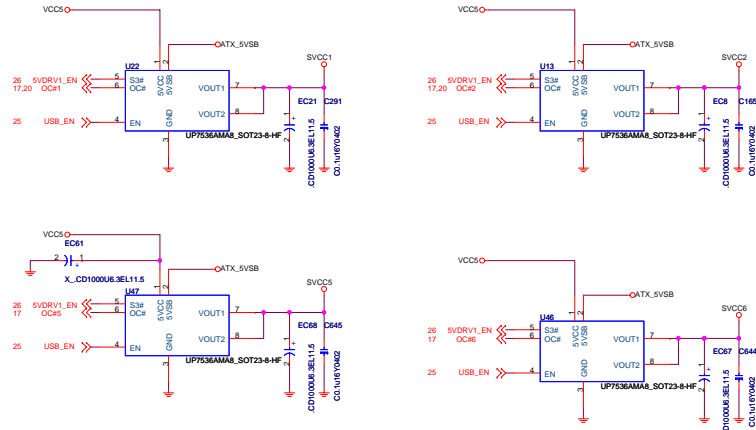
USB 3.0 trace length
Front pin header within 3.5''

USB 3.0 trace length
Rear connector within 8''

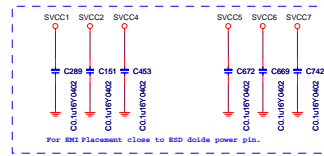
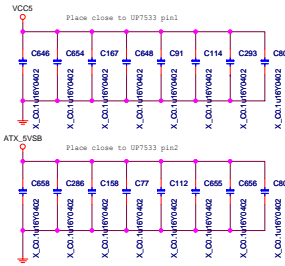
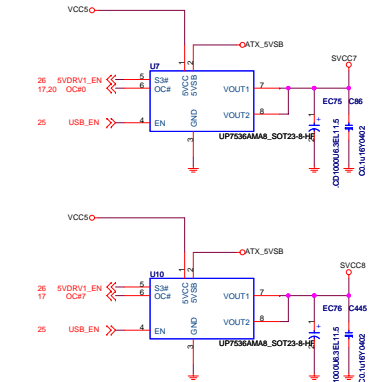
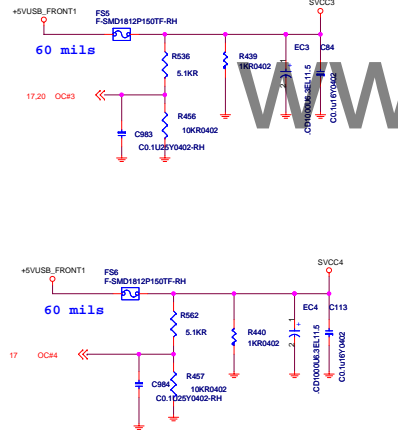
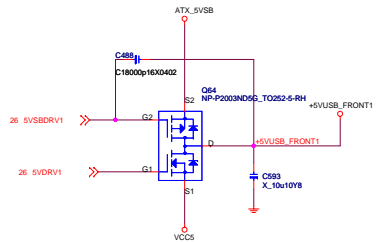


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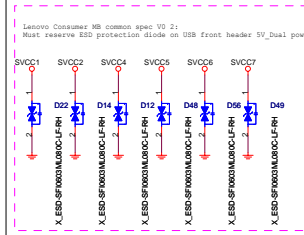
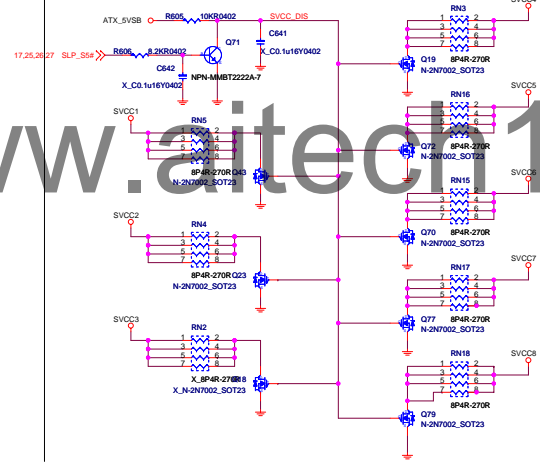
USB 2.0 0.5A port port



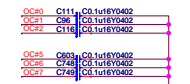
USB 3.0 0.9A port port



USB power discharge circuit

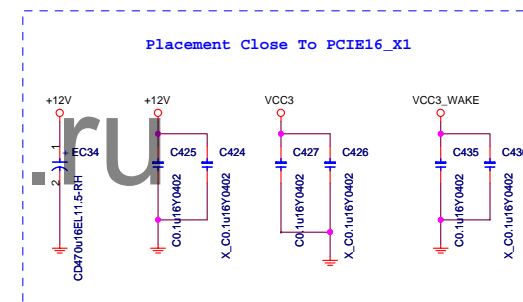
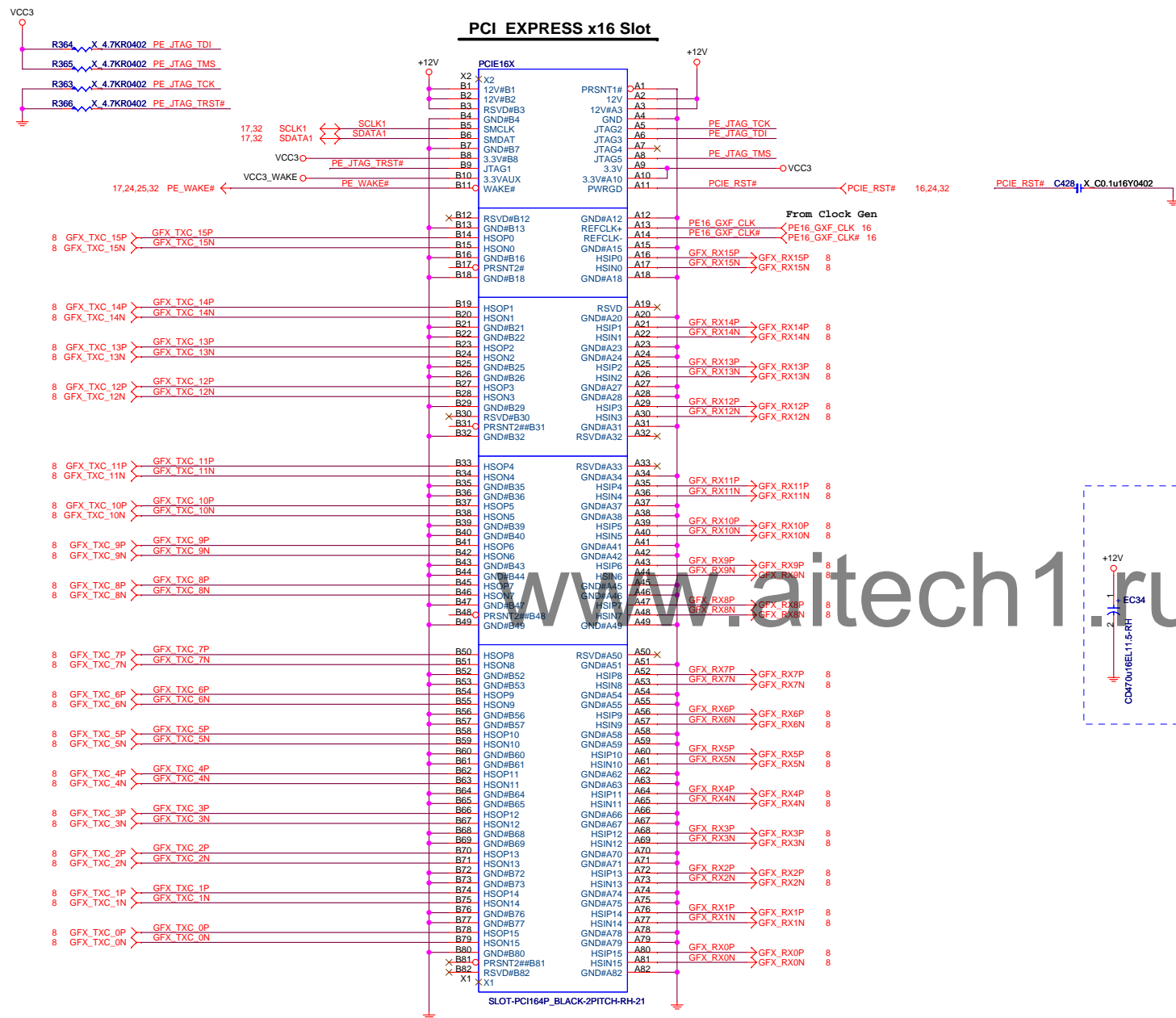


Use low-pass filter to prevent glitches during plug/unplug events.

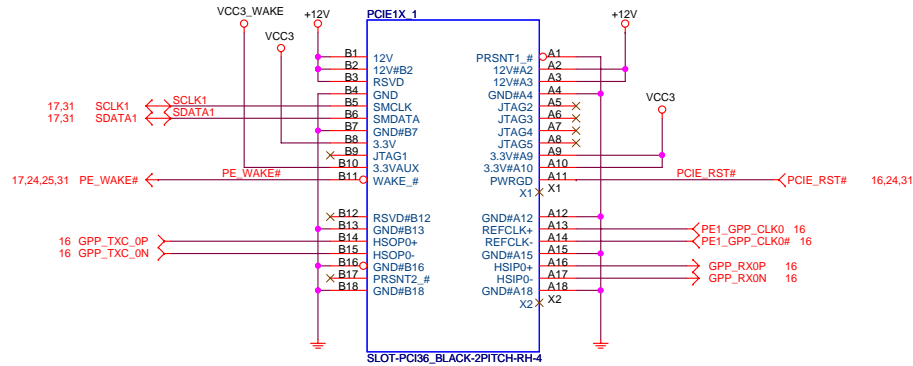


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File: USB POWER/DISCHARGE			
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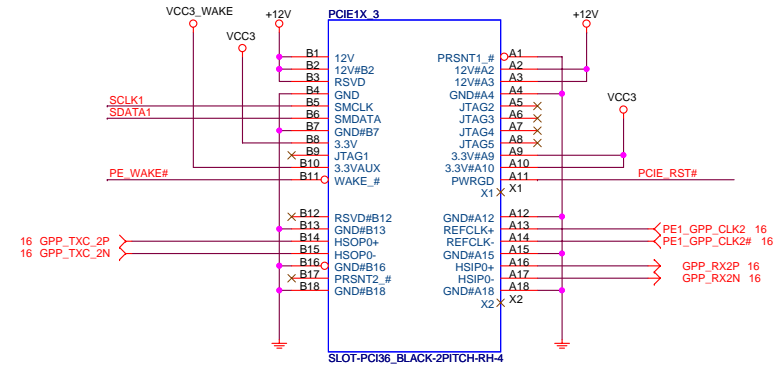
PCI Express Slot x16



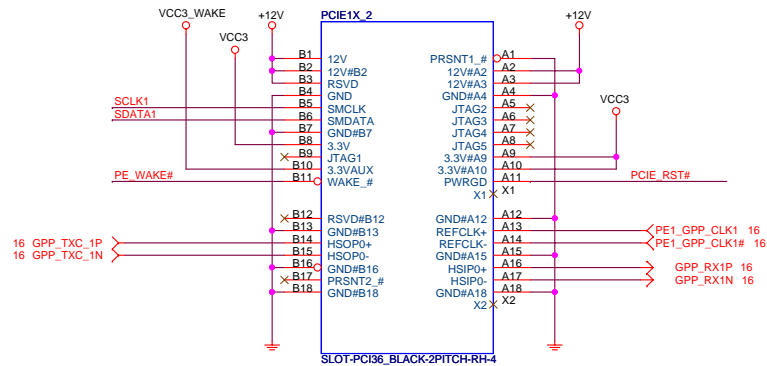
PCI EXPRESS X1 Slot-1



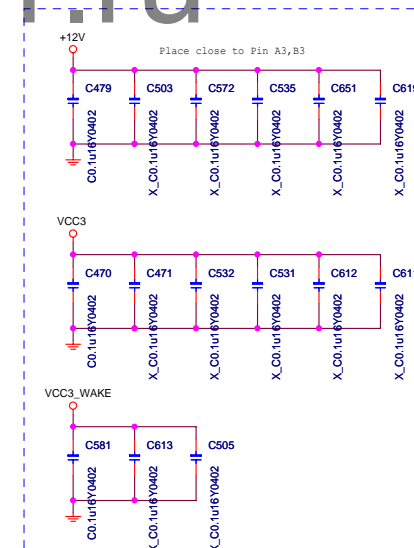
PCI EXPRESS X1 Slot-3



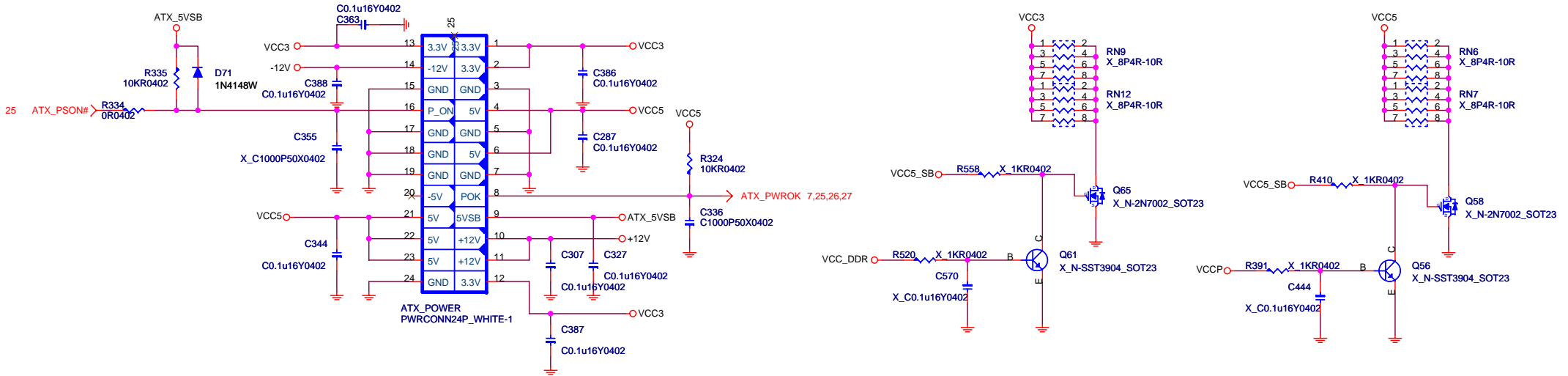
PCI EXPRESS X1 Slot-2



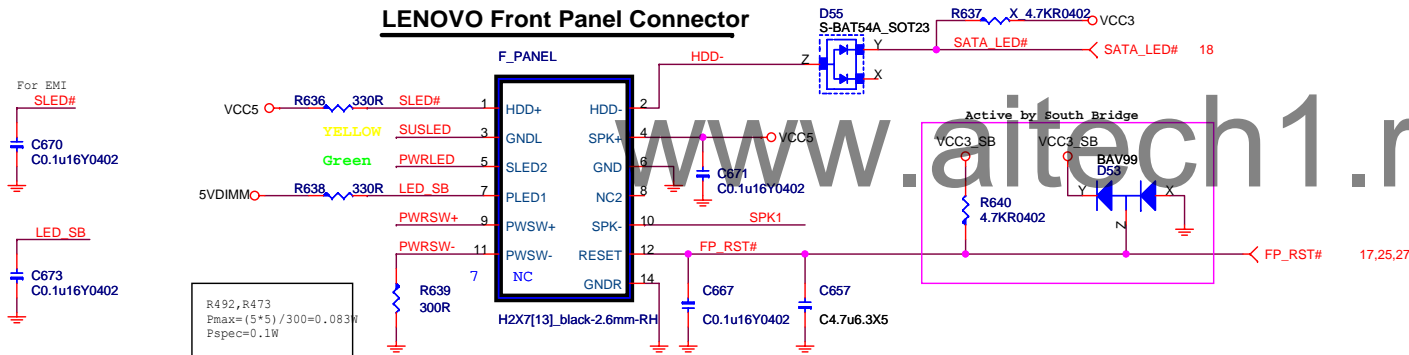
PCIE_RST# C472 X_C0.1u16Y0402



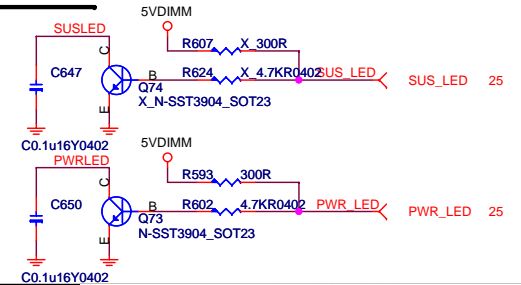
ATX CONNECTOR



LENOVO Front Panel Connector



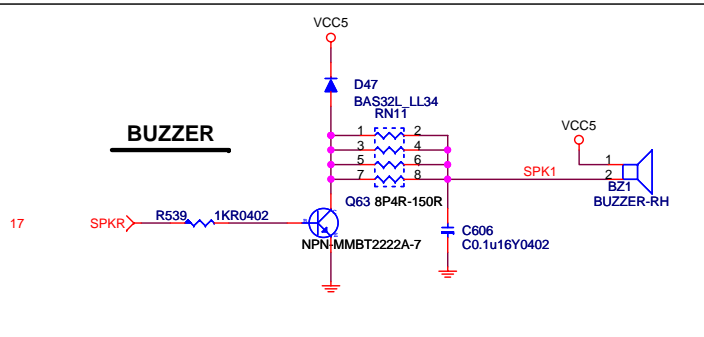
POWER LED



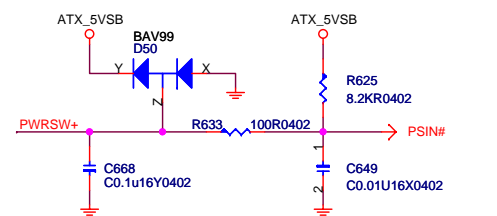
power LED definition

HD (IDE Hard Disk Active LED)		Pin 1: LED anode(+)	Pin 8: LED cathode(-)
(Power LED)		Pin 3: LED cathode(-) (green)	Pin 2: LED cathode(-) (yellow)
Power Switch		Open/Normal Operation	Close: Power on / Off
LED Status (Dual color LED)		Dual Color POWER LED State	
System State		Steady Green	
S0		Green Blinking (frequency is under 1Hz)	
S1		Steady Yellow	
S3		Off	
S4/S5		Off	
Default S5 in lose power		Note series resistor is 330Ω	

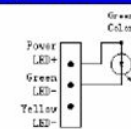
BUZZER



POWER BUTTON

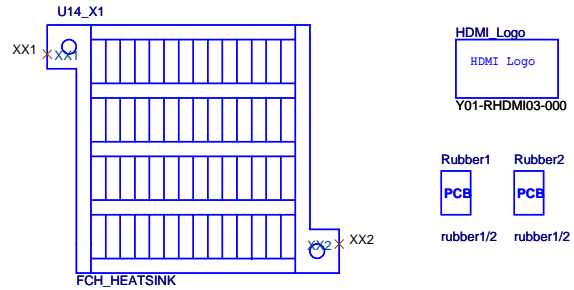


2-pin single color Power LED

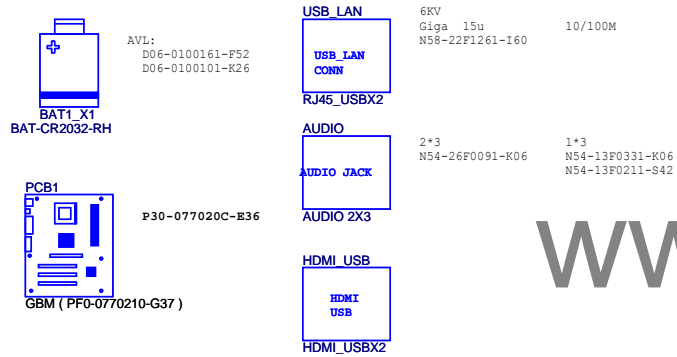


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ATX & FRONT PANEL		
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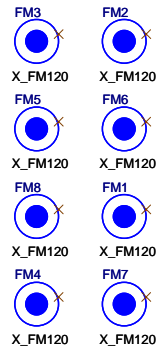
HEAT SINK



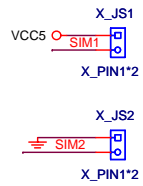
MANUAL PART



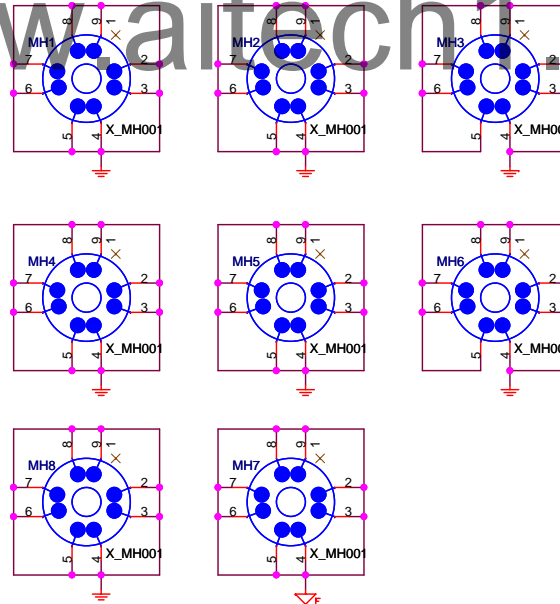
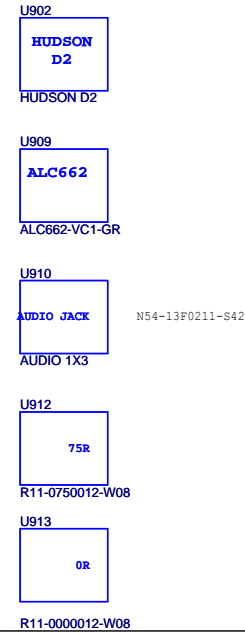
Optics Orientation Holes




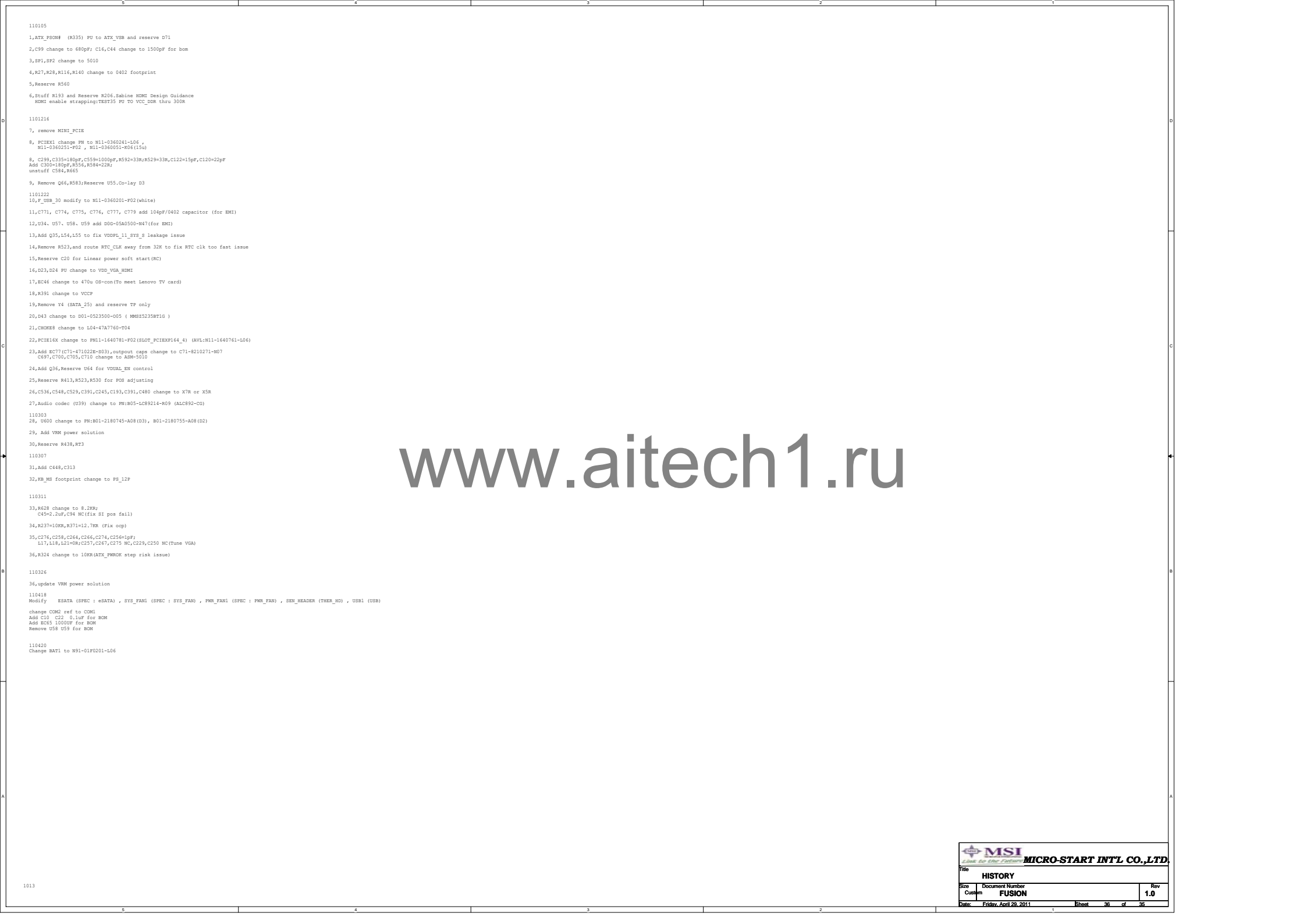
Simulation



Pangkor



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Auto BOM Mnaual		
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110105

- 1,ATX_PSON# (R335) PU to ATX_VSB and reserve D71
- 2,C99 change to 680pf; C16,C44 change to 1500pF for bom
- 3,8P1,8P2 change to 5010
- 4,R27,R28,R116,R140 change to 0402 footprint
- 5,Reserve R560
- 6,Stuff R193 and Reserve R206.Sabine HDMI Design Guidance
HDMI enable strapping;TEST35 PU TO VCC_DDR thru 300K

1101216


- 7, remove MINI_PCIE
- 8, PCIEX1 change PW to W11-0360241-L06 ,
W11-0360251-F02 , W11-0360051-R06(15u)
- 8, C299,C135=180pf,C559=1000pf,R592=33R,R529=33R,C122=15pf,C120=22pf
Add C300=180pf,R556,R584=22R;
unstuff C584,R645
- 9, Remove Q64,R583;Reserve U55.Co-Lay D3
- 1101222
- 10,F_USB_30 modify to W11-0360201-F02(white)
- 11,C771, C774, C775, C776, C777, C779 add 104pf/0402 capacitor (for EMI)
- 12,U34, U57, U58, U59 add DOG-05A0500-H47(for EMI)
- 13,Add Q35,I54,I55 to fix VDDPFL11_SYS_8 leakage issue
- 14,Remove R523,and route RTC CLK away from 32K to fix RTC clk too fast issue
- 15,Reserve C20 for linear power soft start(RC)
- 16,D23,D24 PU change to VDD_VGA_HDMI
- 17,EC46 change to 470u OS-con(To meet Lenovo TV card)
- 18,R391 change to VCCP
- 19,Remove Y4 (SATA_25) and reserve TF only
- 20,D43 change to D01-0523500-O05 (MMS25235BTIG)
- 21,CHOME8 change to L04-47A7760-T04
- 22,PCIE16X change to PH11-1640781-F02(SLOT_PCIEXP164_4) (AVL:W11-1640761-L06)
- 23,Add EC77(C71-4710228-R03),outport caps change to C71-R210271-N07
C697,C700,C705,C710 change to A8M-S010
- 24,Add Q36,Reserve U64 for VDDUAL_EN control
- 25,Reserve R413,R523,R530 for POS adjusting
- 26,C536,C548,C529,C391,C245,C193,C391,C480 change to X7R or X5R
- 27,Audio codec (U39) change to PH:R05-LC89214-R09 (ALC892-CG)

- 110303
- 28, U600 change to PH:R01-2180745-A08(D3), R01-2180755-A08(D2)
- 29, Add VRM power solution
- 30,Reserve R438,RT3
- 110307
- 31,Add C448,C313
- 32,XB_MS footprint change to PS_12P
- 110311
- 33,R628 change to 8.2Kv;
C45=2.2uF,C94 NC(fix SI pos fail)
- 34,R237=10Kv,R371=12.7Kv (Fix ocp)
- 35,C776,C259,C364,C386,C774,C266=1pf;
L17,L18,L21=0v,C257,C267,C275 NC,C229,C250 NC(Tune VGA)
- 36,R324 change to 10Kv(ATX_PWRONK step risk issue)

- 110326
- 36,update VRM power solution
- 110418
- Modify ESATA (SPEC : eSATA) , SYS_FAN1 (SPEC : SYS_FAN) , PWR_FAN1 (SPEC : PWR_FAN) , SEN_HEADER (THIR_SD) , USB1 (USB)
- change COM2 ref to COM1
- Add C10 C22 0.1uF for BOM
- Add EC65 1000UF for BOM
- Remove U58 U59 for BOM

- 110420
- Change BAT1 to M91-01P0201-L06

1013

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